Welcome to the Memory Technology, Design and Testing Workshop (MTDT'09)!

Over the past couple of years, the semiconductor memory, especially DRAM, industry has been undergoing an agonizing downturn, with a scale never seen before. This is partly caused by the financial tsunami triggered by the subprime mortgage delinquencies and foreclosures in the United States. Over-supply leading to cut-throat competition is another culprit. Last but not least, technology is no longer a scarce resource, so the average selling price (ASP) of semiconductor chips will continue to drop, and smaller companies in all segments of the value chain are likely to suffer more frequently in the future. Restructuring of the industry seems inevitable, and is under way. For researchers and engineers staying in this area, there is no other choice but to continue improving our competitiveness—technical depth and differentiation. This is achieved by continued investment in R&D, and exchange results and ideas in a technical forum such as the MTDT.

We managed to form a strong and interesting program this year, albeit the number of submissions is a little bit lower than before, due to the situation mentioned above. The technical program includes 16 papers covering a broad spectrum of the enabling technologies of memory products, including emerging memory devices, advanced memory devices and circuit design, 3D memory technology, memory modeling and testing, etc. In addition, there will be an embedded talk on “Overview of IEEE P1450.6.2 Standard,” which is for memory modeling in Core Test Language (CTL). Another strong point of this year’s program is that we have more distinguished invited speakers than ever before. The first Keynote Speech will be on “Variation Tolerant SRAM Circuit Design Trend in a Deeper Nanometer-Scale Technology” by Prof. Hiroyuki Yamauchi of Fukuoka Institute of Technology. Dr. Michel Renovell from LIRMM will talk about “Fault-Model vs. Defect-Model Oriented Testing” in the second Keynote Speech. Three Invited Talks will be given by Prof. Ya-Chin King of National Tsing Hua University, Mr. Sreedhar Natarajan of TSMC, and Dr. Sheng-Fu Horng of ITRI, respectively. They will cover timely and interesting topics such as new non-volatile memories, emerging technologies, and 3D integration.

We sincerely hope that you will find this event pleasant and relaxed, while informative and inspiring at the same time.

Welcome to Hsinchu and enjoy!

Cheng Wen Wu,
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Rochit Rajsuman,
San Jose State University
General Co-chairs

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