Welcome to the 2003 IEEE International Workshop on Memory Technology, Design and Testing. This is the eleventh annual meeting of the MTDT workshop. As always, we have an exciting program that is sure to stimulate new ideas and insights across a broad range of topics in memory technology, design and test.

New innovations are stimulated by new and more demanding requirements, so this workshop begins appropriately with a keynote address that focuses on new demands placed on memory by future applications. The keynote address titled “Platform Architecture and the Persistence of Memory” will be presented by Dr. Christopher Hamlin, Chief Technology Officer, LSI Logic Corporation. Dr. Hamlin has extensive experience in leading-edge semiconductor systems applications including storage, communications, and personal computers. This system’s perspective enables him to provide useful insights into memory requirements and future trends that will impact significantly on future memory development work.

The theme of applications requirements and technology capabilities that drive memory innovation are continued in the regular paper sessions including topics such as application specific DRAMs and the ITRS Memory Roadmap. Other papers address important practical matters such as optimal spare utilization for memory repair and reduction of test time. Some papers address topics that most of us have never thought about such as a simulation model for the chalcogenide phase-change memory cell. Design topics include DRAM, EEPROM, and SRAM. Continuing the fine tradition established for this workshop over many years, we have an excellent series of papers on memory test, fault analysis, and verification. In total we have fourteen papers this year with a good mix between contributions from academia (8) and industry (6).

Panel discussions are always interesting and stimulate good discussions. This year we have a panel of experts in BIST who will address the question of what are the major challenges remaining for memory BIST – are there any unsolved problems left? A second panel of experts will assess Embedded DRAM – has EDRAM finally arrived? These panel discussions together with the regular presentations combine to make a compelling program for everyone involved in memory development.

We would like to thank the authors and presenters for putting forth the extra preparation effort and for raising interesting topics to spark meaningful discussions. We all extend our thanks and deep appreciation to members of the Steering, Organizing and Program Committees who have put in extra effort to make MTDT 2003 a success. We also thank the TTTC’s Memory Testing TAC and the Solid State Circuits Society for their continued support and we heartily thank the IEEE CS Test Technology Technical Council (TTTC) and the VLSI Technical Committee for agreeing to sponsor this event.

Of course it is the informal discussions among attendees and authors that make the MTDT workshop special. Thanks to all the attendees whose broad range of experience and knowledge and active participation in this workshop make it a rewarding experience for everyone.

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