FLASH MEMORY TECHNOLOGY - A REVIEW

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ABSTRACT

Since the first flash memory patent issued on October 6, 1987, flash memory’s multiple useful characteristics, including nonvolatility, in-circuit reprogrammability, low power consumption, and high density, have led it to become the fastest growing memory segment in recent years. Mobile computing and communication have driven the demand for flash memories. Nascent applications, such as digital cameras, personal digital assistants (PDA), digital telephone answering devices (DTAD) are expected to further add to growth in flash memory demand.

Typically, flash memories are descendants of EPROM or EEPROM technologies and therefore many similarities in the architecture and operation can be noticed. As in the case of EPROMs, flash devices based on NOR architecture and the hot-electron injection mechanism for programming still dominate the marketplace. To provide erasability, the Fowler-Nordheim tunneling mechanism is typically employed. However, booming demand for flash memory has set-off a ferment of new architectures, cell structures, and manufacturing processes. For mass storage applications, NAND architecture is emerging as a contender. AND and DiNOR (Divided bit-line NOR) architectures have also emerged, each having their own advantages and disadvantages. Requirements on low power, low voltages, and higher densities have led to the development of devices which use Fowler-Nordheim tunneling for both programming and erasing. Multilevel
cells which allow storage of more than one bit of data per cell are also drawing a lot of attention.

As in the case of EPROMs, flash devices started out using two power supplies, one supply voltage for read operation, and a higher voltage for programming. However, the clear trend is towards the use of single-voltage supply. For example, in the case of single-voltage NOR based flash devices from AMD, a positive bias is applied to the source, and a negative voltage is generated internally to be applied to the gate. Similarly, for single-voltage NAND devices, an on-chip charge pump generates the necessary high positive voltage from the supply, to be applied during programming. Intel uses a different approach for its NOR based flash devices and calls it Smart-Voltage technology, in which the devices can be adapted to both single- and dual-voltage supply based systems. To accommodate single-voltage and dual-voltage supplies used by different suppliers, JEDEC has defined pinouts for flash memories in which Vpp pin could be either a 'No Connect' or indeed a high voltage pin required for dual-supply devices. Although at present, a majority of the flash memory devices are for 5V systems, new devices which operate at 2.7V are emerging, with 1.8V devices on the horizon.

Flash memories have unique quality and reliability testing issues. Besides memory related issues such as data retention, cycling endurance, cell disturbs, and erase control, flash devices need to be tested for proper functioning of an embedded state machine. As a result, flash memories present a unique challenge to build both analog and digital testability on chip. Testability tools typically include direct memory access to each memory cell with fast, parallel characterization capability, various stress modes to detect weak cells, data retention tests, program verify tests, as well as host of built-in self-tests for the sequential logic.

In this paper, we will review the history of flash memory development, the physics behind the operation of flash memory, various technological approaches, testing issues, and the future anticipated developments for flash memories.