Giga-bit DRAM Trend

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Abstract

DRAM's have been achieving higher and higher memory capacity by
reducing the device sizes and complicating the memory cell structures. At
present, 64M's are available in the market and 1G's are under development in
many semiconductor companies. Some early 1G chips were presented at the
ISSCC (International Solid State Circuits Conference) last year for the first
time. DRAM's have been also getting faster and faster as the generation has
proceeded by taking an advantage of device miniaturization as well as
adopting new circuit designs, such as Synchronous DRAM and Rambus
technologies. Many questions have been recently raised, however, including
the limit of existing memory cell technologies, how to improve speed to catch
up the processor operation without blowing up the power consumption, how to
realize a system that does not require as large amount of memory as the most
advanced DRAM's can provide by a single chip but requires very high data
rate and performance, and so on. Test time/cost reduction is also an issue.

In this presentation, I will review the state of the art DRAM technologies,
functions, and circuit design topics. Trench and stacked cell technologies for
1G DRAM's will be compared. Different DRAM functions will be reviewed and
their performances will be compared. I would also like to explore some of the
issues and questions and to review some ideas recently published intending to
solve these issues. The DRAM and Logic merged technology, which is
presently a very hot topic in the industry and getting more and more popular,
will be discussed as a candidate to provide fairly small amount of memory but
high performance. Future DRAM trends from technology, function, application
and other points of view, will be briefly summarized.