Message from the Program Chair

Welcome to the Third IEEE International Workshop on Memory Technology, Design and Testing. The informal discussion sessions held during the last two workshops proved to be quite successful, and expert presentations, such as the evening panel discussions on selected topics, have been very popular. Further, a survey of the attendees revealed that short technical sessions with plenty of time for discussions, and a couple of detailed presentations is the desired format for the workshop. Keeping all this in mind, the technical program committee is pleased to present this year’s program.

As always, this workshop encompasses two days. The first day starts with the keynote speech on the challenge of merged memory logic by Betty Prince, and also has two technical sessions and one tutorial session. The technical sessions are on the subjects of role of simulation in memory design and bridging faults and Iddq testing. The tutorial session on testing random access memories will be held by Kewal Saluja and Pinaki Mazumder. The second day has four sessions: memory built-in self-test, application specific memory design, advance memory architecture, and new topics in memory testing.

Due to the limited time of a two day format, we were not able to accommodate all submissions. The program committee strived to select the best papers on the subject, and we hope the subject matter and quality of the presentation included in the workshop will be of interest to all attendees.

On behalf of the program committee, I would like to thank all the authors who submitted their work for this workshop. I would also like to express my sincere appreciation to all the member of the program committee and the reviewers for their time and effort in organizing the program and selecting the papers.

Kamal Rajkanan  
Program Chair