MP3 Portable Player System-level Glue Logic on FPGA

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Abstract

Microelectronics systems design is a collaborative, multidisciplinary activity, involving the combined efforts of system architects, circuit designers, device engineers, software developers, and process engineers. There is a need for educational programs in microelectronics particularly at undergraduate level that prepare engineers for the semiconductor industry. This paper is an out-come from postgraduate course project, focusing on the design of MP3 system-level glue logic required to interface and manage the memory and I/O devices. The design has been implemented and verified on a Spartan-II xc2s50 2.5V FPGA.

1. Introduction

Downloading audio from the internet has dramatically increased over the last decade. Limited bandwidth and storage capacity has driven the development of several compression standards, e.g., WMA, AAC, MP3, etc. One of the most successful is MP3, due to early standardization and relatively high compression ratio and good audio fidelity. MP3 portable players are the trend in music-listening technology. These players do not include any mechanical movements, thereby making them ideal for listening to music during any type of activity. As with any portable, battery-operated device, power dissipation must be minimized. The Spartan-II 2.5V Field-Programmable Gate Array family gives users high performance with extremely low power dissipation, abundant logic resources, and a rich feature set, all at an exceptionally low price which makes them ideal for this project. This design uses a 2.5V xc2s50 Spartan-II FPGA to implement the complex MP3 system-level glue logic required to interface and manage the memory and I/O devices. This article describes design overview and hardware implementation of an MP3 system-level glue logic targeting FPGA. The following sections provide basic information about the MP3 format together with implementation details. The development has been performed in a project course. Design modeling has been done on a VHDL framework provided by the course supervisor. The implementation work was completed in 12 weeks.

2. The MP3 format

MP3 (MPEG-I Audio Layer-3) is a method of compressing audio files. The encoder uses a psychoacoustic model utilizing two major concepts: Thresholding and masking. Thresholding exploits the fact that human hearing is less sensitive in the higher frequency range. This means that higher frequencies can be compressed to a higher extent than lower frequencies. The encoder also reduces temporal redundancies by masking out low amplitude frequencies if a dominant is present. By using these techniques, the encoder achieves a compression ratio of about 12:1, using a bit rate of 128 kbit/s.

3. Design overview

The block diagram of the FPGA MP3 portable player is shown in figure 1. It supports graphical user interface and LCD display, parallel port interface for...
downloading MP3 data from PC and flash bank to store downloaded MP3 data.

Figure 2 shows an overview of the architecture implemented in the Spartan-II FPGA. The architecture consists of Main Control Logic, Parallel Port Interface, Flash Control, User Interface Control, I²C Master and power management.

4. FPGA Implementation

The resource utilization on the Spartan-II xc2s50 FPGA are reported in Table I. In total, 31% of the FPGA slices, 12% of the Flip-flops, 28% of the 4-input lookup tables are used in the implementation. Total equivalent gate count for the design is 4522. Table I presents the computation time for the different sub-blocks if a 24 MHz system clock is used. The total time required for the MP3 data processing is 104.08nsec, which indicates that the design can run on a lower clock frequency or that resource sharing can be explored in the design. The design can be improved by utilizing resource sharing among sub-blocks. However both power and area should be considered during such a process. Xilinx WebPACK ISE 5.2 is used for design entry, synthesis and implementation whereas ModelSim XE 5.6e is used to simulate behavioral and post-place and route VHDL model. Figure 3 shows the FPGA development and verification board on which the design has been implemented.

<table>
<thead>
<tr>
<th>Block</th>
<th>Slices</th>
<th>Eq. Gate count</th>
<th>Computation Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Control Logic</td>
<td>12%</td>
<td>1698</td>
<td>41.9nsec</td>
</tr>
<tr>
<td>Parallel Port Interface</td>
<td>1%</td>
<td>88</td>
<td>5nsec</td>
</tr>
<tr>
<td>Flash Control</td>
<td>10%</td>
<td>1302</td>
<td>23.33nsec</td>
</tr>
<tr>
<td>User Interface Control</td>
<td>4%</td>
<td>700</td>
<td>20.35nsec</td>
</tr>
<tr>
<td>I²C Master</td>
<td>3%</td>
<td>650</td>
<td>10.12nsec</td>
</tr>
<tr>
<td>Power Management</td>
<td>1%</td>
<td>84</td>
<td>3.38nsec</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>31%</strong></td>
<td><strong>4522</strong></td>
<td><strong>104.08nsec</strong></td>
</tr>
</tbody>
</table>

5. Conclusion

A FPGA implementation of MP3 portable player glue logic architecture has been presented. This design illustrates how Spartan-II FPGA can be used to provide time-to-market advantages in high volume consumer applications. In this application, the Spartan-II FPGA is used as a cost-effective and low power consuming device compared to processor-based MP3 portable player. This design also allows field upgrade flexibility, in a market where standards and protocols are still evolving. The power consumption is 11.36mW at 2.5 V and 24 MHz.

References

