A DOT1 & DOT4 MOSIS - Compatible Library
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Abstract
There exists a lack of balance between design and testing topics in microelectronic curricula. However, boundary scan as a virtual probe presents an opportunity to teach testing and design for testability in such a curriculum. This effort is facilitated by the use of IEEE standards, universal acceptance in industry, and the availability of low cost test equipment. This paper introduces a library of boundary scan components based on the IEEE standards. The library is being verified using the AMI 0.5 micron 40 pin Tiny Chip VLSI device fabricated through MOSIS services.

1. Introduction
The original boundary scan standard IEEE 1149.1 (commonly referred to as DOT1) is widely accepted [1] whereas its mixed signal extension IEEE 1149.4 (DOT4) has not yet gained a foothold in industry. Commercial DOT4 devices are scarce and there are even fewer academic counterparts. To help in the investigation of the feasibility of DOT4 and to give students an in-depth look at the standard, design libraries have been developed at the University of New Hampshire (UNH). This activity is a part of a broader strategy to introduce testing in the microelectronic curriculum at UNH [2], [3]. The library has been created by two competitive teams of students taking an introductory VLSI course [4]. The two teams were lead by two graduate students, the co-authors of this paper. The rest of the paper describes the boundary scan program at UNH followed by some examples of library modules which were developed. The libraries were developed using the Mentor Graphics ASIC Design Kit (ADK) [5].

2. Boundary Scan in VLSI Curriculum
The current DOT4 experience at UNH is in its 3rd generation. It originated with the evaluation of the DOT4 device from Panasonic [6]. An industrial MCT2020 tester will be available as a tool for testing the DOT4 designs when they come back from fabrication. Besides the VLSI course a testing course is offered with a substantial ingredient of boundary scan [2], [3].

3. Library Development
The libraries were developed using the Mentor Graphics ASIC Design Kit as previously mentioned. Since this is a first course in VLSI design there was a fairly steep learning curve to overcome before any of the real design work on the final project could begin. The design tools were introduced through progressive labs while the students conducted research into their respective modules. In order to keep progress on schedule students and their project leaders were required to compose a timeline for their design. During the semester there were several design reviews during which the students presented their current progress in front of the class and then submitted an updated timeline.

The goal of the project was to implement a library of high-level modules that could be distributed among other educational institutions and have these modules integrated into a single working device to be fabricated through MOSIS and tested in the following semester for validation.

The DOT1 library contains the following cells:
• TAP Controller
• Output MUX
• Instruction Register
• Bypass Register

<table>
<thead>
<tr>
<th>TAP CONTROLLER</th>
<th>VDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>SHIFTDR</td>
<td>5V</td>
</tr>
<tr>
<td>CLOCKDR</td>
<td>Max</td>
</tr>
<tr>
<td>UPDATEDR</td>
<td>250 MHz</td>
</tr>
<tr>
<td>SHIFTIR</td>
<td>Dissipated</td>
</tr>
<tr>
<td>CLOCKIR</td>
<td>power</td>
</tr>
<tr>
<td>UPDATEDIR</td>
<td>19.4 mW</td>
</tr>
</tbody>
</table>

Figure 1. A sample module.

Above is a simplified sample of a module from the DOT1 library. The complete format also includes signal timing information, a schematic diagram, and a layout graphic with dimensions.
The DOT4 library contains the following additional cells:
- Analog Switch (A CMOS transmission gate formatted as a standard cell).
- ABM
- TBIC

5. Overall Design

During the design process the team leaders were prompted to encourage progress by requiring certain information necessary to the overall design completion, such as a block box of their module to determine signal requirements and an estimate of their layout dimensions for floorplanning.

![Sample floorplan](image)

Figure 2. Sample floorplan

After the modules were completed the team leaders integrated the design, placed it in a padframe, and prepared the design for submission to MOSIS.

![Completed layout](image)

Figure 3. A completed layout inside of a padframe.

The final design was simulated after being placed in the padframe and found to operate at 166 MHz. A number of debug signals have been brought out to pads so that the operation of individual modules can also be confirmed.

6. Summary

Currently, the designs have been submitted through MOSIS for fabrication and they are expected to be delivered back in March 2003 for verification and testing. The verification results will be known at the time of the MSE’2003. After verification the library will be made available online.

Boundary scan based initiatives appears to be one of the most promising approaches to restore the balance among technology, system development, and testing. However, the limits and potentials of boundary scan still need to be investigated. For example, a synergy between boundary scan and BIST has proven to be very successful. The fundamental observation is that boundary scan is not just a testing technique, but an attractive alternative to measurement and health monitoring in microelectronic systems.

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References