Educational Use of MOSIS

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Abstract

This paper summarizes and comments on the NSF report “Integration of Education and Research in Microelectronics”. MOSIS is the premier NSF grant highlighting the integration of education and research, affecting a broad section of US Computer Engineering programs. An analysis of the MOSIS Project reports for 1995 has been published [1] and its salient points are summarized here.

Introduction

On March 29, 1996 a workshop was held at NSF to assess the status and future trends of the educational use of MOSIS (Metal-Oxide Semiconductor Implementation Service) [1], which has been credited as a crucial element for excellence in computing and communications in the U.S. [2].

The vision for Educational MOSIS [3] is:

Educate students who can use the paradigm of design, simulate, design-for-test, build and test (as opposed to just design, build and test) to create microelectronic systems, not just integrated circuits, of sufficient quality that the global competitiveness of U.S. industry will be continued and enhanced.

The following principle implements the vision:

Rapid prototyping of microelectronic systems should be an integral part of the education process since students must have the experience of taking a design from initial specifications to a working implementation.

The wide-spread availability of VLSI design realization results from two key developments: 1. the understanding that microelectronic design is largely an exercise in scaleable polygonal component layouts [4]; and 2. the definition of a common data format for defining the circuit design to the fabricator [the CIF data format].

Background

MOSIS has been funded by the Advanced Research Projects Agency since 1981, later jointly by ARPA and the National Science Foundation. Over 25,000 chips have been completed.

The educational use of MOSIS is about 10% of the total budget of MOSIS. Educational designs from classes are about 50% of all fabricated chips. NSF supports beginning and advanced classes. Classes are allocated funds to fabricate 2 um CMOS TinyChips with an area of about 2500 um by 2500 um, enough space for over 4000 transistors. The complexity of such a design exceeds any other design students would otherwise find in college.

Normally funds are allocated is based on one TinyChip per two students for Beginning Classes, and one TinyChip per student for Advanced Classes.

A design project fabricated by MOSIS includes a report. In January 1995 a new database was established for Project reports. The following data is for January 1, 1995 through January 24, 1996.

At the beginning of FY 1995 there were 288 educational accounts, some inactive. Active were 110 Beginning Class accounts (4038 students); 77 Advanced Class accounts (950 students).

It is estimated that 40% of all USA Computer Engineering students were involved.

The number of designs submitted for fabrication were: 948 from Beginning Classes, 238 from Advanced Classes. 556 chips were reported tested, for a report-rate of about 50%. About half of these chips were designed in 1994, and many chips fabricated later are yet to be tested. About 70% of the chips meet or exceed design specifications.

The average cost for a Beginning Class design was $500. For Advanced Classes the budget is one TinyChip per student, but often larger chips are fabricated; the average cost per completed design was $1100. About 53% of the requested budget was used in Advanced Classes, and about 40% in Beginning Classes.

The average time for submission of a design to completion of the report is 23 weeks. There is an inherent two-week inaccuracy in this: fabrication time is taken to be the last day of the month.

Findings

General. MOSIS is the premier NSF grant in the integration of education and research.

Project Precis. The Project Reports show a wide range of application for these chips, including simple counting circuits, modest microprocessors, various instruments and sensors, communication...
and biomedical devices, as well as various computer hardware sections.

Project Ideas. Often class designs are very similar, perhaps duplicates, even in classes located half-way across the country.

Design and Verification Tools. All classes use extensive CAD tools. Many are in the public domain (for example MAGiC), others are commercial packages ranging from extensive and expensive (for example Verilog) to modest (such as Tanner Tools.) Difficulties in verification include parasitic diodes, insufficient ground and power.

Test Procedures. The degree to which testing is included in the design phases depends largely on the individual instructor. There is a need to acquaint instructors with Design-for-Test ideas, the need for extensive testing, and dynamic tests.

Test Equipment. Test jigs and test instruments for functional (In/Out bit streams), for speed, rise/fall time and load tests; reliable high-speed clocks are needed. In many schools the teaching functions rely heavily on research instrumentation.

Instructor Training. New instructors need help; class success rate depends strongly on the instructor. The original training tapes from Cal Tech and Xerox are still a valued resource, but they need to be updated.

Virtual Prototyping. Some schools do only intensive simulation tests. Only about 40% of the Beginning Class designs, and 53% of the Advanced Class designs are submitted for fabrication.

Simulation tools have become more accurate, signals can be ever more accurately calculated; a design's success/failure can be accurately assessed.

Recommendations

The most important recommendations were:

1. Educational-MOSIS needs to be continued, since it has become an essential part of all Computer Engineering educational efforts.

2. Training courses for instructors would be very helpful if VLSI start-up classes, or a video-taped version, would be available with updated resource materials and representative complete designs.

3. Educational-MOSIS Retrospective. A careful retrospective study of the impact of MOSIS should document the anecdotal stories about Educational MOSIS and enterprises that sprang from it.

4. Finer-line Geometries. To make recently-available library-based design tools more widely useful, especially for Beginning Classes, easier access to finer geometries is indicated.

5. Increased Freedom of Fabrication Choices. Instructors should be given more freedom in choosing chip sizes and be allowed to include in their class accounts other MOSIS-supplied services.

6. Design-for-test. Incentives should be made to have each design go through a rigorous Verification and Validation test.

7. Virtual Prototyping. Emphasis should be placed on VP, rather than allowing a design & try-if-it-works approach. One could thus teach a deeper understanding of the VLSI realization cycle.

Observations

Design is details-of-chip oriented, with little system orientation. Need a higher-level circuit/system description, which includes consideration of system aspects: reliability, testability, redundancy for every ab initio design.

VHDL [5], and a layer above VHDL, should be the basic description from which conventional CIF files are extracted. This level of description should force the use of provably-correct building blocks, and sound system engineering principles, including testability and system redundancy.

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References


