Table of Contents

Message from the IEEE MCSoC-15 Honorary Chairs ................................................................. ix
Message from the IEEE MCSoC-15 General Chair, and Organization and Steering Committee Chair ....................................................................................................................... x
Message from the IEEE MCSoC-15 Program Co-Chairs ................................................................................................................................. xi
Organizing Committee .................................................................................................................. xii
Program Committee ................................................................................................................... xiv
Invited Speakers .......................................................................................................................... xvii

General Issues in Many-core Programming and Programmability
An Enhanced Profiling Framework for the Analysis and Development of Parallel Primitives for GPUs ................................................................................................................................. 1
Nicola Bombieri, Federico Busato, and Franco Fummi
Managing the Latency of Data-Dependent Tasks in Embedded Streaming Applications ......................... 9
Xuan Khanh Do, Stephane Louise, and Albert Cohen
Measuring Predictability of Nvidia’s GPU Schedulers: Application to the Summation Problem ................................................................................................................................. 17
David Defour

Methods and Tools for Efficient Architectural Design I
Hierarchical Library Based Power Estimator for Versatile FPGAs ................................................................................................................................. 25
Hao Liang, Yi-Chung Chen, Tao Luo, Wei Zhang, Hai Li, and Bingsheng He
A Scalable and Fast Microprocessor Design Space Exploration Methodology ........................................ 33
Lei Wang, YuXing Tang, Yu Deng, Fangyan Qin, Qiang Dou, Guangda Zhang, and Feipeng Zhang
Expandable Chip Stacking Method for Many-core Architectures Consisting of Tiny Chips

Hiroshi Nakahara, Tomoya Ozaki, Hiroki Matsutani, Michihiro Koibuchi, and Hideharu Amano

**Embedded Multicore/Many-core Architectures**

FACE: Fast and Customizable Sorting Accelerator for Heterogeneous Many-core Systems

Ryohei Kobayashi and Kenji Kise

Why Race-to-Finish is Energy-Inefficient for Continuous Multimedia Workloads

Kristoffer Robin Stokke, Håkon Kvalse Stensland, Pål Halvorsen, and Carsten Griwodz

Reconfigurable IBM PC Compatible SoC for Computer Architecture Education and Research

Eri Ogawa, Yuki Matsuda, Tomohiro Misono, Ryohei Kobayashi, and Kenji Kise

A CGRA-Based Approach for Accelerating Convolutional Neural Networks

Masakazu Tanomoto, Shinya Takamaeda-Yamazaki, Jun Yao, and Yasuhiro Nakashima

**Programming Techniques for Embedded and Parallel Architectures**

FPU Speedup Estimation for Task Placement Optimization on Asymmetric Multicore Designs

Alexandre Aminot, Yves Lhuillier, Andrea Castagnetti, and Henri-Pierre Charles

On the Load Balancing Techniques for GPU Applications Based on Prefix-Scan

Federico Busato and Nicola Bombieri

Abstracting Parallel Programming and Its Analysis Towards Framework Independent Development

Oliver Jakob Arndt, Tile Lefherz, and Holger Blume


Asieh Salehi Fathabadi, Luis Alfonso Maeda-Nunez, Michael J. Butler, Bashir M. Al-Hashimi, and Geoff V. Merrett

**Multi/Many-core Applications**

GPU Particle Swarm Optimization Applied to Travelling Salesman Problem

Olfa Bali, Walid Elloumi, Pavel Krömer, and Adel M. Alimi

Energy-Aware Bio-signal Compressed Sensing Reconstruction: FOCUSS on the WBSN-Gateway

Daniele Bortolotti, Andrea Bartolini, Mauro Mangia, Riccardo Rovatti, Gianluca Setti, and Luca Benini

Top-Down Profiling of Application Specific Many-core Neuromorphic Platforms

Gianvito Urgese, Francesco Barchi, and Enrico Macii
Dynamic Mechanisms for Performance Improvement

Predictable Application Mapping for Manycore Real-Time and Cyber-Physical Systems ................................................................. 135

Anil Kanduri, Amir-Mohammad Rahmani, Pasi Liljeberg, and Hannu Tenhunen

Automatic Runtime Customization for Variability Awareness on Multicore Platforms .............................................................. 143

Gasser Ayad, Ramakrishna Nittala, and Romain Lemaire

Dynamic VC Organization for Efficient NoC Communication ........................................................................................................ 151

Masoud Oveis-Gharan and Gul N. Khan

A Performance Prediction for Automatic Placement of Heterogeneous Workloads on Many-cores ..................................................... 159

Nicolas Benoit and Stephane Louise

Memory Management and Design

Adaptive Time-Based Least Memory Intensive Scheduling .............................................................................................................. 167

Amr Saleh Elhelw, Ali El-Moursy, and Hossam Ali Hassan Fahmy

Comparison of Shared and Private L1 Data Memories for an Embedded MPSoC in 28nm FD-SOI ............................................................ 175

Gregor Sievers, Julian Dabeckow, Johannes Ax, Martin Flaschkamp, Wayne Kelly, Thorsten Jungeblut, Mario Porrmann, and Ulrich Rückert

Lighting the Dark-Silicon 3D Chip Multi-processors by Exploiting Heterogeneity in Cache Hierarchy .................................................. 182

Ashkan Sadeghi, Kaamran Raahemifar, Mahmood Fathy, and Arghavan Asad

Memory Access Analysis of Many-core System with Abundant Bandwidth ....................................................................................... 187

Chuan Tang, Dan Liu, Zuocheng Xing, Peng Yang, Zhe Wang, and Jiang Xu

Auto-Tuning for Multicore and GPU

CLTune: A Generic Auto-Tuner for OpenCL Kernels .................................................................................................................... 195

Cedric Nugteren and Valeriu Codreanu

Enhancement of Incremental Performance Parameter Estimation on ppOpen-AT ............................................................................... 203

Riku Murata, Jun Irie, Akihiro Fujii, Teruo Tanaka, and Takahiro Katagiri

Improving Auto-Tuning Convergence Times with Dynamically Generated Predictive Performance Models ........................................ 211

James Price and Simon McIntosh-Smith

The Approximate Discrete Radon Transform: A Case Study in Auto-Tuning of OpenCL Implementations .......................................... 219

H. Martin Bücker, Ralf Seidler, David Neuhäuser, and Tobias Beier
# Multicore/Many-core Interconnection Networks

**FTTDOR: Microring Fault-resilient Optical Router for Reliable Optical Network-on-Chip Systems** ................................................................. 227

*Michael Conrad Meyer, Akram Ben Ahmed, Yuichi Okuyama, and Abderazek Ben Abdallah*

**Contention-Free Routing for Hybrid Photonic Mesh-Based Network-on-Chip Systems** ................................................................. 235

*Achraf Ben Ahmed, Yuichi Okuyama, and Abderazek Ben Abdallah*

**Communication Aware Design Method for Optical Network-on-Chip** ........................................................................................................... 243

*Johanna Sepúlveda, Sebastien Le Beux, Jiating Luo, Cedric Killian, Daniel Chillet, Hui Li, Ian O’Connor, and Olivier Sentieys*

**On the Design of Reliable Hybrid Wired-Wireless Network-on-Chip Architectures** ................................................................. 251

*Michael Opoku Agyeman, Ji-Xiang Wan, Quoc-Tuan Vien, Wen Zong, Alex Yakovlev, Kenneth Tong, and Terrence Mak*

**3D Shared Bus Architecture Using Inductive Coupling Interconnect** ........................................................................................................... 259

*Akio Nomura, Yu Fujita, Hiroki Matsutani, and Hideharu Amano*

# On-chip Communication Architectures for Multi-core and Many-core Systems

**Cross by Pass-Mesh Architecture for On-chip Communication** ........................................................................................................... 267

*Usman Ali Gulzari, Sheraz Anjum, and Shahrukh Agha*

**Implementation and Modeling for High-performance I/O Hub Used in SPARC M7 Processor-Based Servers** ........................................................................................................... 275

*John Feehrer, Jeffry Hughes, Hugh Kurth, David Pabisz, and Peter Yakutis*

**Accelerated On-chip Communication Test Methodology Using a Novel High-Level Fault Model** ........................................................................................................... 283

*Elmira Karimi, Mohammad-Hashem Haghiy, Amir-Mohammad Rahmani, Mahmoud Tabandeh, Pasi Liljeberg, and Zainalabedin Navabi*

# Methods and Tools for Efficient Architectural Design II

**ADRENALINE: An OpenVX Environment to Optimize Embedded Vision Applications on Many-core Accelerators** ........................................................................................................... 289

*Giuseppe Tagliavini, Germain Haugou, Andrea Marongiu, and Luca Benini*

**Enabling Scalable and Fine-Grained Nested Parallelism on Embedded Many-cores** ........................................................................................................... 297

*Alessandro Capotondi, Andrea Marongiu, and Luca Benini*

**The Network Performance Analysis Platform and Its Application to Network Buffer Evaluation of the Embedded System** ........................................................................................................... 305

*Yuichi Sakurai, Kenichi Shimbo, Tadanobu Toba, and Hideki Osaka*

# Author Index ........................................................................................................... 313