IEEE-488.2 COMMUNICATIONS BY INFRARED WIRELESS LINK

M.J. Betancor¹, J. Martín¹, J. Rivero¹, V.M. Melián¹, F.J. Gabiola², F.J. López-Hernández²

¹ Univ. de Las Palmas de G.C.
Dpt. Electrónica y Telecomunicación
E.T.S.I. Telecomunicación
Campus Universitario de Tafira.
35017 - LAS PALMAS. SPAIN
Fax: +34 28 451243

² Univ. Politécnica de Madrid
Dpt. Tecnología Fotónica
E.T.S.I. Telecomunicación.
Ciudad Universitaria
28040 -MADRID. SPAIN
Fax: +34 1 3367319

Abstract - In this paper we present the design of an IEEE-488.2 (GPIB) system which uses a wireless infrared link. The wireless link provided mobility into laboratories where GPIB instrumentation is used. The data transmission is by serial link. This type of systems presents some advantages over conventional cable systems. Besides, when we use IRED, the radiation is negligible for the users and harmless. The opto-electrical GPIB interface uses commercial IREDS and photodiodes.

I. INTRODUCTION

Systems which use wireless infrared present some advantages against conventional cable systems [1]: they are lower costs, allow for total mobility of the terminal equipment, the signal is limited to the volume where it is produced (soundproofing as opposed to similar systems in nearby volumes) and no special training is required for their installation. Last years some groups have been working in this kind of communications and several works have been presented at conferences [2][3][4][5].

The designed GPIB system has two different blocks: extension circuitry and serial communications circuitry.

The electrical-to-optical interface and vice versa use an IRED and a photodiode respectively. The electronic circuits associated with optoelectronics devices have been developed too. These are an IRED driver and a photodiode amplifier. The scheme for them are similar to other IR systems. [2][3]

The block diagram is shown in figure 1. Part of the circuits have been made with ASICs techniques to minimize interface and reduce power consumption.

Because frequency modulation enhances signal-to-noise ratio, FSK (Frequency Shift Keying) scheme is used. That is two frequencies for transmission.

The system is full compatible with IEEE-488.1, IEEE-488.2 and IEC 625-1 standards.

II. TECHNIQUES USED

The IEEE 488-1978 Std, IEEE Standard Digital Interface for Programmable Instrumentation, deals with systems that use a byte-serial bit-parallel means to transfer digital data among a group of instruments and system components. This designed extender is compatible with all revisions of the IEEE-488 standard.

This extender system removes the restrictions on cable length and devices loading imposed by the IEEE-488 standard. The IEEE-488 standard specifies that the total cable length cannot exceed 20 meters and the maximum number of devices is 15. With the extender system, up to 15 devices, including an Extender unit, can be interconnected by GPIB interface cables to an extender unit.

The system is transparent to software and to data.
buffer. The system expands the maximum number of devices up to 28, and the maximum lengths to a room volume or one kilometer (point-to-point link). Figure 1 shows a block diagram of the system.

The GPIB extender uses ASIC techniques. The system can be reduced to two EPLDs: Master and Slave. Master EPLD includes generation of system clocks, clock recovery, synchronization, data packing and error detection. Slave EPLD controls PROM.

The Interface Bus transceivers used are monolithic, high-speed, three-state outputs, low-power Schottky devices. It uses a power up/down disable circuit that provide a glitch-free operation during VCC power-up and power-down. The transceiver provides an interface between EPLDs and CMOS circuits and the IEEE Standard Instrumentation Bus (GPIB). The required bus termination is provided through these interfaces.

The system can work up 500 Kbit per second. The frequencies for mark and space are 2 MHz and 2.5 MHz respectively. The data are sent in packets by infrared wireless link.

The extender unit converts the bit parallel GPIB protocol into a bit serial stream that is packaging into a 26 bit data frame and transmitted over a wireless infrared link to the remote extender unit. At the other end of the link, the other extender unit unpacks the 26 bit data frame and put them on the GPIB bus. The entire range of GPIB functions may be extended to remote sites.

The system uses a 4-bit CRC (cyclical redundancy check) code to detect errors. Packets received with an error are rejected and automatically a code error is transmitted to the remote system and last packet is retransmitted.

Figure 2 shows a block diagram of the extender. The ability to respond to Parallel Poll commands is maintained, although the timing of the parallel poll response will be slightly altered due to the transmission delay in an extender system like this. If line is down, the system resets itself and then begins executing the link establishment protocol.

III. GPIB EXTENDER CIRCUITRY

The system has three main sections; the interface circuitry, the monitor circuitry and the communication circuitry.
III.1. INTERFACE CIRCUITRY.

The interface circuitry is intended as the bidirectional bus transceiver that interfaces between the CMOS logic, in which operates the system's circuitry, and the GPIB bus. The required bus termination is provided by the interface circuitry.

The Interface Bus transceivers used are monolithic, high-speed, three-state outputs, low-power Schottky devices. It uses a power up/down disable circuit that provides a glitch-free operation during VCC power-up and power-down. The transceiver provides a interface between EPLDs and CMOS circuits and the IEEE Standard Instrumentation Bus (GPIB).

Interface circuitry provides three-state drivers with a 48mA of sink current (100mA maximum), as required in higher speed operation, with the exception that DIO1-8 use open-collector drivers configuration for parallel polling applications. All the receivers have 3-state outputs to present a high impedance to the terminal when disabled.

System can be configured in a point-to-point configured system, a star configuration or tandem configuration.

III.2. MONITOR CIRCUITRY

This circuitry monitors the local GPIB states and converts the signals monitored, after these are processed, into T signals (T signals are referred to signal that are ready to transmitted). T signals are then driven into the packet generator in order to be packets with the data signal, 3 internal command bits (needed to transmit some internal control messages to the remote extender) and the 3-bit CRC. Then a start bit and a stop bit are added to complete the 26-bit packet to be transmitted. The packet configuration is as follows.

```
+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+
|  STB  |  IFC  |  REN  |  ATN  |  SRQ  |  EDI  |  DAV  |
|-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------|
|  KIF  |  DAC  |  KFP  |  DR-1 |  C3-1 |  CRC4 |  SPB  |
```

This section is composed of the following blocks (figure 2):

III.2.1. Power on reset and Delay for Self-Test: When the unit is powered on, a reset pulse clears all circuitry to an initialized state, all the flip-flops in the EPLDs are cleared to the initial state; this is very important in order to the right operation of the system and the FF included in the EPLDs.

After the system reset, the extender is in a passive state. The extender remains in this state until communication is established with the remote extender; while the extender is in the passive state, interface circuitry remains in high impedance (three-state) not driving anything on the GPIB.
After the link establishment protocol is made, the unit is able to monitor the local GPIB state, and receive packets from the remote GPIB extender.

III.2.2. System and Active Controller Detection: This block monitors the location of the System Controller and the location of the Active Controller. Operation of System Controller detection and Active Controller detection is as follows. System Controller Detection monitors the location of the System Controller with the state of signals T.IFC, T.REN, R.IFC and R.REN (T refers to signals to be transmitted, and R to signals received). When IFC or REN true is received from local System Controller then is assumed that the location of System Controller is in the local extender, and flag LSCA (Local System Controller Active) becomes true. Then T.IFC and T.REN are then sent to the remote extender unit. If R.IFC or R.REN is received true from remote extender controller RSCA is sent true (Remote System Controller Active), LSCA is cleared and R.IFC and R.REN are driven onto the local GPIB Bus. Active Controller Detection monitors the location of the Active Controller. The location of the Active Controller is determined by sensing the location of ATN. ATN indicated where is the Active Controller and it is indicated by flags LACA and RACA, when ATN is received from the local unit LACA is sent true and RACA is cleared, and viceversa. The true state of the flag allows the local or remote unit to receive SRQ from the remote unit if LACA is true and from the local unit if RACA is true.

III.2.3. Source Handshake Detection: The location of the source Handshake is determined by the location of DAV. When DAV is received from the Local GPIB Bus, the LSH (Local System Handshake) becomes true and DAV is sent to the remote unit on the T.DAV signal. When R.DAV is received from the remote unit RSH (remote System Handshake) then becomes true.

III.2.4. 4-Bit CRC Generator: This block received 24-bit to be transmitted from the "Parallel to Serial Converter" block and given out the same 24-bit added 4-bit CRC.

III.2.5. Packet Generator and Parallel to Serial Converter: Signals from System and Active Controller Detection, Source Handshake Detection, Parallel Poll Control and DIO1.8, are parallel to serial converted and then sent into the 4-bit CRC Generator block. Bits from 4-bit CRC Generator are added with one start bit and one stop bit to get a data packet.

III.2.6. Latch: Packet to be transmitted is latched and transmitted to the remote unit. If an error is detected on the remote unit, the last packet in the latch is retransmitted. After the packet is transmitted, the extender unit has a timeout circuitry that provided a delay which corresponds to twice the propagation delay of the link for a packet transmitted. If a packet is not received within this time, a packet is received indicating that an error is detected in the last packet received in remote unit, the local extender unit goes into a error state, this error state is indicated in the external Error LED indicator.

III.2.7. Synchronization: Gives the signals for the other blocks.

III.2.8. Transmission Clock Generator and Start-Stop Bit Generator: Gives the several clocks needed for transmission system. The start-stop bit is generated in this block and sent to Serial-to-Parallel Converter.

III.2.9. Memory Controller: This blocks controls the EEPROM for patterns self-test.

III.2.10. Link Establishment: The link between extender units is active using a continuous packets transmission protocol. Each of two units transmits a packet as soon as a packet is received, and so communication between the extenders is continuos.

III.2.11. Clock Recovery: The clocks are recovered from received packet with this block. This circuitry synchronizes the reception internal clock with received data. This is for transmission clock of 500 Kbits/sec and a delay of 60 nsec (worst case).

III.2.12. Packet Check: The received packet structure is checked in this block. If the format is unknow, the unit sends a command to remote to send packet again.

III.2.13. Error Detection 4-bit CRC: When start and stop bits are removed from received packet, CRC is checked. If an error is detected the packets will be sent again.

III.2.14. Serial to Parallel Converter: This block converts serial data to parallel format to send them to GPIB bus.

III.2.15. Parallel Poll: When the unit detects ATN and EOI simultaneously asserted on the local bus, the parallel poll-in-progress state becomes true and T.EOI is transmitted to the remote side along with T.ATN.
T.EOI and T.ATN are transmitted to the remote unit a parallel poll response is returned from the remote unit, even if local ATN and EOI signals become false. NRFD is asserted on the local bus during the parallel poll.

III.2.16. Data Flow: This block controls data flow all time.

III.3 COMMUNICATION CIRCUITRY

III.3.1. FSK Modulator: This block modulates the data to send them to remote unit. The modulation is FSK (Frequency Shift Keying) implemented with a VCO.

III.3.2. IRED Driver: is a high speed TTL circuit. It converts electrical signal in optical signal. The IRED output is transmitted by wireless to optical receiver.

III.3.3. Photodiode Amplifier: The preamplifier is a transimpedance amplifier with bipolar TRTs that allows a wide bandwidth and dynamic range and an acceptable sensibility.

III.3.4. Filter: This block filters the signal received from remote unit. It is a band pass active filter.

III.3.4. FSK Demodulator and Regenerator: The output of Filter is demodulated for this block and then regenerated using a high-speed comparator.

IV. IRED DRIVER AND PHOTODIODE PREAMPLIFIER

The circuits for IRED driver and photodiode preamplifier are shown in figures 3 and 4. IRED Driver is a high speed TTL circuit [2] [3] (figure 4). Photodetector used was pin-photodiode. The preamplifier is a transimpedance amplifier with bipolar TRT that allows a wide bandwidth and dynamic range and an acceptable sensibility [2] [6] (figure 4). After this circuit is a high speed differential comparator that delivers TTL level data.

V. CONCLUSIONS

This paper presents the design of a compatible IEEE-488.1 and IEEE-488.2 extender that uses infrared link to avoid cable in GPIB-laboratories. The design uses serial communications for data and control signals. This kind of extenders allow full mobility in cable laboratories or the control of instrumentation in next buildings by infrared wireless point-to-point link.

ACKNOWLEDGMENT

This work has been supported by Comisión Interministerial de Ciencia y Tecnología (CICYT). Project number: TIC91-1222-CE

REFERENCES


