MESSAGE FROM THE LATS2015 CHAIRS

On behalf of the Organizing and Program Committees, the General and Program Chairs warmly welcome all the participants to the 16th IEEE Latin-American Test Symposium (LATS2015). This year the conference is held in Puerto Vallarta (Mexico). LATS, (previously named Latin-American Test Workshop - LATW) is a recognized forum for test and fault tolerance professionals and technologists from all over the world, in particular from Latin America, to present and discuss various aspects of system, board, and component testing and fault-tolerance with design, manufacturing and field considerations in mind.

This year the LATS2015 offers an excellent Technical Program, which is composed of 35 regular papers presentations, one Special Session, one poster session, one Keynote address, one TTEP Tutorial and four Invited Talks. The regular paper presentations cover contributions on fault simulation and modeling, automatic test generation, analog mixed signal test, memory testing and fault injection, System-on-chip test, software based fault tolerance, built-in self-test, Issues on EMC, EMI and Radiation, design verification and validation and fault tolerance architectures. The Special Session is focus on Issues in Electronic Design Automation: Tolerance Analysis and Design Verification. The poster session covers aspects of robustness analysis, analog testing and reliability issues. In this opportunity we will have an up to date Keynote Address titled “Top 10 Semiconductor Trends: ... that are changing how we Design, Manufacture, Test & Deliver High-Quality ICs” given by Phil Nigh from IBM. An interesting TTEP tutorial is offered titled “Test & Yield Challenges in Today’s Technology Nodes” given by Yervant Zorian from Synopsys. Four Invited talks in highly important novel topics are also offered: "Sub-10nm Technology Nodes: Design and Test Challenges” given by Kaushik Roy from Purdue University, “Scan Based Two-Pattern Tests: Should They Target Opens Instead of TDFs?” given by Adit Singh from Auburn University, “System on a Chip Security Fundamentals” given by Ismael Rangel from Intel and “In-field test of safety-critical systems: is functional test a feasible solution?” given by Matteo Sonza Reorda from Politecnico di Torino.

The realization of LATS2015 could not be possible without the work of very dedicated volunteers. We deeply and sincerely thank the members of the various committees, the authors, the reviewers, the session chairs, the secretariat and the technical support personnel for their valuable contributions. Finally, we would also like to acknowledge the financial sponsorship given by the National Institute for Astrophysics, Optics and Electronics (INAOE). We also thank the technical Co-sponsorship of the IEEE, the Test Technology Technical Council and the IEEE Council on Electronic Design Automatic (CEDA).

We do hope that you take profit of the LATS2015 Technical Program which has been carefully prepared for you. We also hope that you might enjoy Puerto Vallarta, a city located in the Pacific Coast of Mexico within a large bay called Banderas Bay.

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