Abstract

Silicon Interposer is the new PCB where silicon of different process technologies (like logic, DRAM, analog, etc.) can be bonded onto and integrated into the same package. Silicon interposer has microbumps on one side and flipchip (C4) bumps on the other, and signal on one side are connected to the other with TSV (Through Silicon Vias). Die to die interconnects are just wires from one microbump to another without connecting to any C4 on the bottom side. Essentially, these are tiny PCBs that have their dimensions shrink by 100x. Conceptually PCB essentially are just interconnects so testing really are just open/short and maybe leakage, i.e., ONLY if you can connect (or probe) to the microbumps. However, at 40-50um pitch, they are almost half the pitch of the most advanced flipchip bump technology with tens of thousands of microbumps in a typical application. The tight pitch and mass quantity of microbumps would drive for new probe technologies (read, more expensive) and complex test optimization at the ATE side. There is also no transistors (nor diodes) on this new PCB, so all you learnt about DFT is out the window. At the same time, it is expected to have zero test cost (as yield should be high). Some in the industry have suggested “Pretty Good Interposer”, only testing for systematics and not defects. Is, “pretty good”, good enough to stand in for “known good”? It all depends on what you put on these interposers and potentially yield loss can kill a product’s viability. This talk will try to elaborate the challenges and will try to propose new test methods for testing these new, miniature PCB.