Trading-Off On-Die Observability for Cache Minimum Supply Voltage Reduction in System-on-Chip (SoC) Processors
Invited Abstract

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Abstract

Circuit techniques for reducing the minimum supply voltage ($V_{\text{MIN}}$) of last-level and intermediate static random-access memory (SRAM) caches enhance processor energy efficiency. For the first time at a 16nm technology node, projections of a high-density 6-transistor SRAM bit cell indicate that the $V_{\text{MIN}}$ of a 4Mb or larger cache exceeds the maximum supply voltage ($V_{\text{MAX}}$) for reliability. Thus, circuit techniques for cache $V_{\text{MIN}}$ reduction are transitioning from an energy-efficient solution to a requirement for cache functionality. Traditionally, error-correcting codes (ECC) such as single-error correction, double-error detection (SECDED) aim to protect the cache operation from radiation-induced soft errors. Moreover, during the qualification of a system-on-chip (SoC) processor, test engineers monitor the rate of correctable cache errors from SECDED for observing the on-die interactions between integrated components (e.g., CPU, GPU, DSP, etc.). This presentation highlights the opportunity to exploit ECC for reducing the cache $V_{\text{MIN}}$ while simultaneously providing coverage for radiation-induced soft errors. Silicon test-chip measurements from a 7Mb data cache in a 20nm technology demonstrate a $V_{\text{MIN}}$ reduction of 19% from SECDED. In addition, silicon measurements provide a salient insight in that only 0.12% of the cache words contain an error when operating at the cache $V_{\text{MIN}}$ with SECDED. Therefore, SECDED improves $V_{\text{MIN}}$ by 19% while maintaining 99.88% coverage for radiation-induced soft errors. In applying SECDED for a lower cache $V_{\text{MIN}}$, the rate of correctable errors exponentially increases, thus eliminating a useful metric for on-die observability. The presentation concludes by offering alternative solutions for on-die observability.