Abstract

Volume manufacturing often highlights aspects of post silicon data analysis that are otherwise overlooked. Yield-overkill, in simple terms, can be defined as failing perfectly good/functional devices due to device testability. Such yield overkill is often linked to tight test conditions using advanced fault models and functional tests. Transition Delay Fault Model (TDF) is one such widely used fault model to detect speed related manufacturing defects. “How do I know whether a given TDF fallout is real or an artifact of some test/process/design combination that may never ever get exercised in the system (functional testing)?”. We deal with analyzing such situations on a daily basis. Often the decisions are more scientific, where a successful PFA of a TDF failure may reveal process issues (thinned oxide, weak metal, broken via etc) but many a times could be a ghost hunt – burning debug cycles (vector, design, system correlation, FA etc) and eventually living with the yield overkill. With complexities in semiconductor design and manufacturing ever increasing (faster designs in small process nodes with increasing quality requirements) solving such real time low level problems is going to be critical for companies to maintain their profitability. The EDA industry has come a long way in abstracting advance fault models – however, the EDA industry needs to go further and address the fine subtleties of design/test/process interactions ensuring rightful balance between cost and quality.