Some Burning Issues that Justify Power-Aware DFT

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1. Dimensions of the Problem
There is no question that awareness of power dissipation during testing is essential. In fact, there are many levels of awareness with respect to power:

- Measuring power during functional test
- Managing power during structural test
- Testing the power management features
- Testing despite the power management features

The first two fall into the category of managing the high-power aspects of testing; the next two are pertinent to the need to test the low-power aspects of a design. All of these dimensions have an impact on power-aware DFT.

2. High-Power Test Issues
Despite the buzz around low-power test, some of the most interesting issues are still at the high end of the meter.

2.1 Measuring Power and Thermal Specs
For both low-power and high-power designs, the conformance to a power dissipation specification (and the associated thermal design profile) is a key parameter that must be validated prior to shipping a product. Given the nature of IC process variation, there can be a wide distribution of measured power consumption values among defect-free devices, necessitating production test for power on a per-part basis. This requirement has many ramifications on DFT, from the design of on-chip power and temperature monitors to the choice of scan or functional tests to excite the worst-case power conditions to the selection of test equipment (both ATE and probe card hardware) and test application flows to support these measurement conditions [1]. It is important not to ignore these fundamental issues despite all the recent attention to low-power test and power-aware ATPG.

2.2 Managing Structural Test Power Issues
Much has been published about the likelihood of scan test patterns having higher power dissipation (due to their greater switching density) than functional patterns, and DFT unquestionably has been employed to ameliorate this issue. Solutions range from the simplest traditional approach of reducing scan shift frequency in proportion to the increased activity factor, to more sophisticated approaches that reduce IR drop by changing ATPG fill policy or adding idle cycles prior to capture [2] or disabling combinational logic [3], or that mitigate di/dt effects by calibrating clock stretch [4]. Test scheduling (i.e. deciding which components to test concurrently) and scan chain partitioning with associated scan clock gating are other DFT techniques used to manage scan test power, all of which will become more important as test time (and compression) are traded off against test power.

3. Low-Power Test Issues and DFT Solutions
Dealing with the plethora of low-power design techniques has added new challenges for DFT. Testing the logic that comprises the power management hardware can be addressed with standard structural DFT, but testing and calibrating the power monitoring instruments may require analog DFT features. Likewise, verifying the functionality of the fine-grained power gating circuitry (like header or footer transistors) can be impossible without very precise power measurements or special DFT structures. Conversely, the mere presence of power management features (such as voltage islands and automatic clock throttling) can wreak havoc with global test signals and test execution unless DFT is implemented carefully.

Beyond these tactical problems, the fundamental test issues in a low power design are: 1) validating that the actual power consumed in each managed power state meets the specification, and 2) proving the device functions properly through all power state transitions. Without power-aware DFT, these are daunting problems.

4. References