Investment vs. Yield Relationship for Memories and IP in SOC

Joseph A. Reynick

eSilicon Corporation, Allentown, Pennsylvania, USA

Abstract
Today’s large SOC designs are using higher percentages of outsourced IP and manufacturing than in the past. At the same time, native IC yield is shrinking due to higher memory defect densities and higher percentages of memory. Today, memory repair and redundancy, along with ECC methods are the prevalent means for active yield remediation. Methods need to emerge for standard logic. From a business perspective, there is a paradigm shift to outsourcing IP and manufacturing. This raises several important questions. How can yield be maximized? What are the limitations of active yield improvement? What is the fastest path to a solution if there is a yield issue? Who owns the native yield? Who owns the test yield?

1. Introduction
Today’s SOC design and manufacturing teams are spread out geographically, and across many companies. SOC IC’s are collections of:

- Repairable and non-repairable memories;
- IP cores like microprocessors, PLL, DDR, and SerDes;
- Standard cell and IO libraries;
- Random digital logic;

Each of the above components has its own native and tests yields that have to be controlled in order to ensure high quality and predictability, while maintaining competitive IC costs.

Memories tend to have the highest defect densities, and comprise a higher percentage of SOC die area than in the past. This combination means that memories substantially contribute to the native yield of the SOC. As such, active methods are required to boost memory yield, such as soft repair/ECC, hard repair, and firm repair.

The major factors that influence yield include:

- Design: Follow Fab design rules. Use a comprehensive DFT strategy with high fault coverage. Functional validation and timing closure at process corners.

2. Yield - A Shared Challenge

2.1 An Investment in Yield Improvement

eSilicon’s position is that each source in the IC flow needs to take ownership, and guarantee their piece of the yield. This requires nominal capital and NRE investment. Specific recommendations include (in precedence):

- IC Fabs: Detailed Defect Densities for IO’s, standard cell digital logic, memories, and analog logic. Yield related/DFM DRC rules. Low cost Memory/IP/Library test shuttles at process corners, with full qualification. Concise tapeout requirements. Yield guarantees.
- EDA Tools: Push yield related DRC changes back to the physical design stage so that yield, area and performance can be optimized in a single pass.
- Library Vendors: Yield optimized libraries. Include DFT structures/models for IO’s, standard cell logic. Functional verification, corner lot verified timing. ESD/latch-up validation. Design guarantees.
- Memory/Hard IP Providers: Same as library vendors, plus DFT structures such as memory BIST/logic BIST. A Test access strategy. DFT based Diagnostics. Yield optimized IP. Yield/performance tuning logic. Corner lot validation with multiple configurations that are correlated to datasheets. Verified vectors. Integration, validation, and diagnostic tools. Design guarantee
- Core Logic Designers: Integrate memories, IP, and libraries per vendor guidelines. Top-level IP access. Functional verification, as well as SI verified timing.
- IC Vendors: Overall yield coordination. DRC/LVS validation. Yield tracking based on measured test data, including memory repair yields. Concise handoffs. Add DFT structures such as memory BIST/scan/logic BIST/boundary scan. Physical/DFT design guarantee.

2.2 A Quick Recovery

If a yield issue should arise, the ASIC/IC Vendor is looked to as the “general contractor” to identify the problem, coordinate the resolution, and move it into manufacturing. In this role, the IC vendor needs to pull together the various contributors to help ensure a quick recovery, and to equitably assign the costs of any rework to the source of the yield issue.