What do you mean my Board Test stinks?

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Introduction
In printed circuit board manufacturing we have generally talked in terms of yield at the end of the manufacturing line. But as the yields has improved over the last 10-15 years from the mid 80’s to the high 90’s yield has become lest relevant and a real measure of quality of the end product become increasingly important.

Background
Fault coverage is a way of measuring how effectively the test stages are and was very useful in the early 70’s for digital boards when the majority of functional test systems used fault simulators that would model simple stuck at faults on a node. By default shorts and internal digital device faults would also be found.

In the early 90’s In-circuit test systems, with full access to the board under test, could guarantee 100% shorts coverage, measure the quality of analog measurement within tolerance bands and used the simple “stuck at model to determine the digital test coverage for individual devices. By its nature we have less confidence in the quality of tests for large digital devices but device quality was and is high and it was only the programmable devices that gave concern. Full location testing and test generators for PAL’s overcame that problem.

Today with the high yields the problem and view of defects has changed. In-circuit test, which is primarily an electrical test system is still trying to find electrical faults but has focused more on finding manufacturing faults. Automatic Optical Inspection and Automatic X-Ray Inspection has also supplemented In-circuit test. This is due in part to a lack of access but also the accepted spectrum of defects has increased from opens and shorts to potential defects such as lack or excessive solder. Below this we have to look at the type of faults the shorts and opens represents. Shorts can be adjacent pin or far shorts, which are less likely. Opens can be solder opens, broken tracks or ever missing or mis-orientated packages. Device faults can be missing, wrong, faulty and mis-orientated. We now have a larger defect spectrum, which also includes devices that are have no electrical functions such as connectors, strengthens, labels etc, which makes up a complete PCB.

Standards
IPC have done a very good job of defining defects per million opportunities (DPMO) and how to measure it. IPC 7912 (Calculation of DPMO and Manufacturing Indices for Printed Circuit Assemblies) and how that translates to yields within the manufacturing environment with IPC 9261 (In-Process DPMO Estimated Yield for PWA). The main weakness of this approach is that it is a historical model that only deals with faults that can be detected in the manufacturing process. If it not detected then it will never appear in the calculations.

The Real Requirement
The reality is that in the manufacturing environment we really need to understand the defects that may escape from the manufacturing environment and the probability of that fault occurring, not what faults have been detected. Those defects can be real faults or potential defect but the importance of those faults and the probability of them occurring needs to be understood. In some designs, faults, like missing decoupling capacitor can be tolerated but in other high speed designs decoupling capacitors and for example multi power connection (another common redundant defect) need to be present for the design to work at full speed.

What the industry needs is an agreed fault model for a board, that we can overlay DPMO information and estimate the escapes right from the design stage to determine the best inspection strategy. Once we have a test strategy we need to get real detection information in the manufacturing setup to understand what faults can escape into the field. The weighted escapes to the field reflect the potential quality of the final product. This will never be zero but if understood can be traded against the potential impact and cost.

Understanding the weighted faults that can escape is the real measure of the quality of the manufacturing process.