GLAMOROUS ANALOG TESTABILITY – WE ALREADY TEST THEM AND SHIP THEM… SO WHAT IS THE PROBLEM?

Mohamed M. Hafed
DFT MicroSystems Canada Inc.
1450 City Councillors Street, Suite 1000, Montreal, Quebec Canada H3A 2E6
mohamed.hafed@dftmicrosystems.ca, Tel: (514) 878-8271, Fax: (514) 878-9338

Despite historically being one of the first areas to benefit from automation, analog circuit test poses particular challenges to modern test technology. In fact, contemporary analog test seems to represent a niche area for which solutions are always future ones. Yet, analog circuits are being mass-produced at astounding rates (whether within more complex digital IC’s or as purely analog parts). This apparent paradox is addressed in this panel, which adopts a problem-solving approach to defining and addressing the analog test domain. It is the panel’s position that the very definition of everything “analog” has shifted in recent years, and a significant dichotomy between test practitioners and chip manufacturers on the one hand and DFT-providers or researchers on the other exists. For example, a first glance at the global chip market may suggest that the purely “analog” market (e.g. linear components) constitutes a small segment, yet most traditionally digital manufacturers constantly rely on mixed-signal test platforms for production screening (because of the increasing analog nature). Are not all IC’s analog IC’s then? What is more is that these manufacturers continue to ship “mixed-signal ASIC’s” in large volumes, which seems contradictory to most claims that analog testability research is lacking. The first goal of this panel, then, is to define the analog problem space at this point in time, segmenting it according to significance, technological challenge, or market share. A typical question that will be raised is: with the rapid proliferation of mobile/wireless computing, will testing power-management IC’s (or circuits within IC’s) be the biggest challenge, or will it be the radio front-end or the on-board high-speed serial bus? An equally important goal of the panel is to identify current solutions, and to list the precise problems they target. In this context, a typical question may be: is DFT or BIST really the answer, or should the research community focus more on test techniques? As it turns out, the industry is indeed going through a rapid change that is impacting everything from test engineers to test equipment and business models. This, coupled with little investment in the way of analog options in test equipment, is one of the many reasons there is a “problem” in analog testability.

The selection of the panelists was made with the above goals in mind. Specifically, our expert panelists represent chip manufacturers, subcontract manufacturers, and the DFT/test technique research community. Each of the panelists represents different views on the most important analog problems as well as competing views on practical solutions. The outcome of this panel is intended to be a clearer definition of the analog test problem, an evaluation of current testability solutions, and an identification of the most important problems that need to be solved.

Organizer: Mohamed Hafed, DFT Microsystems
Moderator Andre Ivanov, University of British Colombia
Panelists Sandeep Kumar, Agere Systems
Robert Chua, Stats-US
Gordon Roberts, DFT Microsystems
Karim Arabi, PMC-Sierra