New Yield Challenge

Today’s leading-edge semiconductor companies are suffering the growing pain caused by technology discontinuity at 0.13um and below. Traditional yield management is becoming insufficient to address the new problem — “feature-limited” or “design-limited” yield loss (see figure below). If this problem were not addressed timely, it would make no economical sense for the industry to continue investing in 90nm and below processes and 300mm fabs.

When IC feature size becomes significantly smaller than the wavelength of lithography, the process window becomes prohibitively smaller as well. More aggressive RET (reticle enhancement technique) needs to be applied. In other words, more of your layout design needs to be compensated or corrected on masks using OPC (optical proximity correction), which also means your layout design will increasingly affect the quality of OPC.

Currently, OPC quality verification is not an industry standard yet; and OPC-aware layout design is also lack of solutions and methodologies. Primarily, at 0.13um, people still can manage to improve lithography process window for majority of designs, but only to start finding OPC problems at high performance and high complexity designs. Another key reason is that the industry requires a high performance and high capacity tool to handle large OPC database. Today’s commercial ORC tools (optical rule checking), which are used to verify OPC quality, are neither designed to handle large OPC database nor to enable DFM, i.e. “OPC-friendly” designs.

Industry Paradigm Shift

Today, manufacturability is defined by design rules. Fabs are set up this way to take over yield responsibility from design after a clean DRC. However, at 01.3um and below, design and process are so intertwined, designs can significantly impact manufacturing yield. Manufactures start providing design guidelines in addition to traditional design rules. Unfortunately, these gross guidelines are not circuit-specific and lack of quantitative information, often result in larger area and degraded performance.

OPC defects are frequently caused by specific layout design patterns. These layout patterns are simply not “OPC-friendly” for a particular litho process. In such a case, manufactures need to communicate litho restrictions as early as possible to design teams. That means designers cannot wait to fix the problem after tape-out and after mask. They need to “tape-out” much early at cell library and block level, and capture majority of “OPC-unfriendly” layout patterns before the final tape-out.

The industry paradigm has to be changed at 0.13um and below. Process engineers need to proactively engage in design phase and eliminate manufacturing limiting issues as early as possible. They need to provide additional OPC service to enable designers to build manufacturable layout patterns way before final tapeout.

Enabling High-Yield Design

EDA vendors are naturally positioned to take on the challenge to provide the DFM tools to bridge the gap and effectively translate manufacturing knowledge to designers.

To close the loop, the problem can be addressed at two levels — design and verification level. At design level, designers need to make sure that their libraries, IPs and block layouts are “OPC-friendly”. The tools are required to automatically detect and correct these issues based on early manufacturing data. For high-yield designs, layout patterns also need to be proved manufacturable at process corners.

At final tape-out and OPC level, the tools are required to verify full-chip to see if there are any newly created problems in final chip assembly.

Key Requirements for DFM Tools

1. Accurately simulate pattern transferring process
2. High performance to cut verification time from days to hours
3. High capacity to handle tomorrow’s large design with hundreds of Giga bit database
4. Efficient, hierarchical data analysis capability
5. Easy to use by designers (a design tool, not a manufacturing tool)

Summary

Design and manufacturing community must quickly adopt DFM solution and methodology in order to cross the technology "chasm" and continues to push Moore’s Law.