IBIST™ (Interconnect Built-in Self-Test) Architecture and Methodology for PCI Express: Intel’s Next-Generation Test and Validation Methodology for Performance IO

Jay J. Nejedlo, Intel Corporation, Hillsboro, OR, USA
jay.nejedlo@intel.com

Abstract
This paper summarizes the test challenges associated with next-generation platform buses and introduces an Intel-developed technology called IBIST™ (Interconnect Built-In Self-Test) created to meet those challenges. The IBIST™ testing methodology and associated on-die architecture customized for PCI Express (PCIe) interface is described.

This paper was submitted under the ITC Special Board and System Test Call-for-Papers that had an extended due-date. As such, the full text of the paper was not available in time for inclusion in the general volume of the 2003 ITC Proceedings. The full text is available in 2003 ITC Proceedings—Board and System Test Track.