From the viewpoint of a casual observer, it appears that less than 10% of the paper and panel presentations at ITC in the last 10 years have been related to board test. Of those, the majority have focused on boundary scan testing. Note that both IEEE 1149.1 and IEEE 1149.4 are standards for IC’s. Board testing continues to be a significant challenge for producers of both high volume and high complexity PWA’s. The impact of a poor board/system test strategy is felt even more by contract manufacturers. So why is it, then, that board and system test are not receiving more attention at ITC?

A fundamental reason for the apparent lack of interest in board test stems from a long-term belief that full component testing and manufacturing defect testing at the board level should provide adequate yields at board and system level testing. At the board level, manufacturing defect testing (XRAY, AOI, In-circuit test and Boundary-scan test) is well understood. Current technology seems to be adequate to detect most manufacturing defects (shorts, opens, un-installed components, wrong components, mis-oriented components). Hence, the emphasis on component testing over board testing.

This viewpoint is flawed for two reasons. First, newer technologies such as RF, Optical and high speed serial data links are now challenging current manufacturing defect test strategies. Probe access for In-circuit testing is not feasible due to signal integrity issues. Boundary-scan test logic imposes large performance penalties on these high speed circuits and in most cases would be considered impractical for such circuits (although IEEE P1149.6 addresses some of these concerns).

This lack of coverage forces companies to rely on functional test strategies that are less understood and may not provide adequate coverage for manufacturing defects.

The second flaw stems from the belief/requirement that the components are free of defects when they are assembled on to the board. The ever increasing complexity of IC’s are making it more and more difficult to completely verify the design. In fact, board test engineers have always had to deal with some level of chip design issues that have made their way into production. In addition, the size, speed and complexity of IC’s are starting to challenge the capabilities of ATE. Add to that, technologies such as RF where fault modeling is much less understood, and it may be difficult to guarantee high fault coverage in the future. Again, most IC design and coverage problems cannot be detected by manufacturing defect testing and must be addressed by functional testing at the board and system level.

It is important to get a better understanding of board and system level functional testing. Functional testing will become more prevalent in the future because of reduced effectiveness of manufacturing defect testers and increasing complexity of IC’s. Functional testing is the last line of defense for most companies before the product ships to the customer. It is also feedback process for design defects and component defects that were not covered by ATE. In general it is not possible to detect these defects with manufacturing defect testers. Even though board test is not a popular topic at ITC, functional testing will become more prevalent in the future and for this reason there needs to be more research and discussion.