GHz Testing and its Fuzzy Targets

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Our forty-year history in IC testing teaches us that "test problems are eternal and test solutions are temporary." Test technology has never been easy; it just appears that way looking back. The GHz ICs are not just about speed, but the technology properties that come with it. The tiny geometry's that gave us speed also vex us with manufacturing uncertainty. GHz ICs happen to be more sensitive to interactive effects than their ancestors because 100 nm geometry's have more process variance, and the clock period is so small at 200-500 ps. These small clock periods are less forgiving.

Tim Turner of Keithley Instruments test structure department estimates that among the several hundred process steps, there are 10,000 variables that can affect performance [1]. The fishbone diagram of this reality is intricate. A parameter may have a statistical variance that by itself may not cause failure, but can cause failures when combined with the statistical values of other parameters. These are called interactive effects. For example, a statistically larger channel combined with a statistically higher interconnect impedance might cause high-speed failures, but each individual variance may not do so by itself.

ICs are increasingly more sensitive to their power supply voltage and local temperatures. The $F_{\text{max}}$ sensitivity to $V_{\text{DD}}$ at 180 nm, 150 nm, and 130 nm technologies is reported at 200 kHz/mV, 1.8 MHz/mV, and 11.3 MHz/mV [2-4]. The increasing GND bounce and IR drop noise on power lines now impacts IC frequency stability more than before. In addition, the transient heat generated by local circuit activity on the IC further contributes to $F_{\text{max}}$ variation. A final observation is that board power supplies at ±5% accuracy can significantly influence board performance of an IC that was tested to manufacturing test specifications.

Defect detection efficiency suffers for all test methods. $I_{\text{DDQ}}$ and delay fault (DF) test methods are challenged to establish tight test limits in a sea of increased variance. In the GHz environment, doubt exists whether DF testing actually detects many failures related to delay [3]. Data indicate that the DF test is probably the most effective test method for detecting open defects, while $I_{\text{DDQ}}$ remains the most effective test method for detecting bridge defects. There is nothing in the present test suite to replace these methods, so we might predict higher bridge and open defect escapes. The stuck-at fault test is a subset of DF gate level testing. The SAF test has a slow clock rate delivery, requires large data storage, and is the most inefficient defect test. All three tests are used in GHz ICs, but we must be aware of their limitations. The ATE challenge of GHz at-speed testing remains for other to describe.

What do these variables imply for testing GHz ICs? The statistical parameters that we now see demand statistical analysis of test variables, such as $F_{\text{max}}$, temperature, $I_{\text{DDQ}}$, memory access time, and $V_{\text{DD}}$. The test procedure will fail ICs, not on a single test, but on deviations from expected behavior over the full range of data. Multi-parameter testing will become the dominant test paradigm [5].