TEST AND REPAIR OF NON-VOLATILE COMMODITY AND EMBEDDED MEMORIES

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Introduction
Semiconductor memory market has been driven by DRAM. However non-volatile memory market, Flash memory as a representative, is growing remarkably because of its versatile application market such as cellular phone, PC memory card, silicon audio, digital still camera storage, automobile application with MCU and so forth. In terms of testing, it is quite different from DRAM. This will describe the differences, requirements and solution of Flash memory testing from viewpoint of ATE.

Flash Memory Testing and Repair
Regardless of device kinds, test cost minimum is the key word for the testing. In order to achieve it, ATE design must be considered to realize highest throughput and lowest tester cost. Typical DRAM tester is designed based on higher paralleled shared resource architecture. However, Flash memory tester architecture may not be the same. The main reason is Flash memory device characteristics itself. Here it will briefly describe the differences between DRAM and Flash memory testing.

In case of DRAM testing, test time is basically same even if device is good or bad. When we consider functional test time which takes most of percentage of whole memory test, parallel device measurement method saves test cost a lot because of no test time increase even you test many devices in parallel. However Flash memory test time will vary depends on each device characteristics. For example, the time to be programmed or to be erased is different depend on device. In case of shared resource tester, each test time is determined by slowest bit device or fail device.

At front-end test, repair method is also different. In case of DRAM, redundancy structure is more complicated and laser fuse blow method is typically used. Higher throughput repair analyzer is the key for DRAM front-end tester. Flash memory’s case, typically redundancy structure is not so complicated and flash cell itself can be used for address replacement, therefore, so called on line repair, can be done during testing. Flash tester is required to have not only repair analysis but also unique repair address generating capability per device.

As these are described above, Flash memory device behaves more independently than DRAM especially testing point of view. Therefore, tester per DUT type of architecture has more throughput benefit at front-end test even tester cost is considered more expensive than shared resource tester. However, at back-end test, shared resource architecture still have more cost benefit since bad device was already repaired or rejected at the front-end and test time differences per DUT is more less than front-end test.

NAND/AND Flash Device
NAND/AND Flash memory application is more focused on higher density storage market. They also have unique test requirement. NAND/AND device is called "mostly good memory" which means some bad block/sector are allowed as a good device. Tester must maintain each device’s bad block/sector location for go/no-go decision and for masking bad block testing to avoid longer test time.

Embedded Flash Memory
Embedded Flash memory is mostly combined with MCU or ASIC and its flash memory size is still not so large. To test logic and memory function by single tester is questionable in terms of test cost. Test strategy of embedded flash is different depends on manufacturer. For example, if repair is needed, it may be tested with low cost memory tester at front-end and BIST will test flash at back-end with logic tester. Some cases, memory tester may be required to access embedded Flash through logic pins. In this case logic vector generation capability should be equipped to memory tester which will impact tester cost.

Future Requirements
Test requirements of next non-volatile memory, such as FeRAM, MRAM, OUM, are not clear yet. However, it is getting more difficult for ATE maker to design one tester fits all memory devices. ATE maker’s challenge is to realize more flexible features with lowest tester cost. Tester cost impact versus test specifications/functionality needs to be continuously considered. On the other hand, DFT/BIST availability seems to be the key to realize lowest test cost solution in the near future.