Good Scan = Good Quality Level? Well, It Depends…

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What is quality?

Quality can be defined as “a degree of excellence”.† In practice, we use testing as a measure of the outgoing quality of devices. The problem is that there is not a one-to-one correlation between test and quality. Just because a unit is tested doesn’t guarantee that it is defect-free. Similarly, “guaranteed-by-design” functionality, usually isn’t (with no offense intended to the incredibly talented designers out there).

So, what does it mean when we talk about Quality Level? In essence, we are trying to increase our confidence that devices shipped to customers will work as advertised in their application. For existing products, this is relatively straightforward because of the existing history of how the device performed in the field. For new designs, the difficulty lies in trying to predict this confidence level based on simulations and engineering data. Sometimes we can extrapolate from previous generations of a design or other devices which are being manufactured on the same process technology node. But, these alone are not enough to provide a perfect forecast of how the device will succeed. As a result, the usual method of attack is to apply whatever test techniques are available and can be practically implemented for first silicon.

Enter the debate: Scan vs. Functional Test

The tug-of-war between scan protagonists and functional believers has been going on in earnest for a long time now, with little chance of an end anytime soon. Nevertheless, there has been a noticeable shift in the industry over the last few years. Major players who were strongly committed to functional testing (you know who you are) have stood up at conferences and admitted they now rely largely on scan based testing. Moreover, the reports indicate that this has been accomplished with little to no reduction in the quality levels of the devices.

How do we compare functional and scan based testing? There are many criteria, some of which include design impact, tool support, test development cost, and tester hardware requirements. Let’s look at a few other considerations for a typical high-end microprocessor.

- **Test Time.** The execution time required for functional tests as compared to the combination of embedded memory tests and scan tests is fairly even. *Advantage: neither*
- **Test Pattern Reuse.** Functional test patterns generally don’t change for minor silicon revisions. In contrast, scan based patterns must be generated from scratch each time. *Advantage: functional*
- **I/O Modes.** Extensive testing of high speed or multiple frequency I/O buses is not very easy to do with scan based testing. However, some of the newer ac scan methods are trying to address this. *Advantage: functional*
- **Embedded RAMs.** Functional patterns which completely test the memory arrays are often unacceptably lengthy. Scan based access is more predictable, but is not robustly supported by EDA tools. *Advantage: neither*
- **Mission Mode.** Scan based testing just can’t operate the device in mission mode. *Advantage: functional*
- **Debug and Diagnostics.** Functional debug is a nightmare, which means that most of these failures end up in the “unresolved” bucket. Here is a category where scan based testing wins without a doubt – but only if your scan tests catch the failure! *Advantage: scan*
- **Fault Coverage.** Coverage metrics are hard to measure for functional testing but can be empirically derived from DPM levels and no-trouble-found system failures. Scan tools provide statistics, but how accurate are these numbers? *Advantage: scan*

And the winner is…

Testing is not a “one size fits all” solution to assure a certain quality level. Yet the trend is moving towards more structural testing for a reason, and certain devices (especially ASICs) have already made the substantial leap to using predominantly structured testing. As scan techniques advance, it may be that functional testing will become less and less prominent. At the moment there is no clear winner, but the race is on…