ITC 2001 Paper Awards

As part of the process of maintaining and encouraging quality of work written and presented in the technical program, ITC presents awards to authors of selected papers presented at the conference and published in the proceedings. In the process of determining the award-winning papers, the ITC Awards Selection Committee considers reviews and comments from several sources:

- Responses by conference attendees as recorded on the session ratings cards
- Observations and recommendations of the ITC Program Committee

For the 2001 ITC Program Best Paper Award, the Awards Selection Committee has selected:

**Neighbor Selection for Variance Reduction in $I_{DDQ}$ and Other Parametric Data**

*W. Daasch, K. Cota, J. McNames – Portland State University,
R. Madge – LSI Logic*

The subject is nearest-neighbor residual estimates for $I_{DDQ}$ and other test measurements. New data-driven neighborhood selection techniques are demonstrated with robust variance reduction and improved identification of die outliers.

The Awards Selection Committee has also selected for Honorable Mention award:

**Debug Methodology for the McKinley Processor**

*D. Josephson, V. Govan – Hewlett Packard, S. Poehlman – Intel*

International Test Conference congratulates the authors of these papers for their achievements and for the outstanding quality of their work. The $2,000 Best Paper Award and $1,000 Honorable Mention Award and commemorative plaques are presented to the authors at the plenary session of ITC 2002. International Test Conference strongly values the input made by the conference attendees when filling in the session ratings cards. They provide feedback to the Program Committee on the strengths and weaknesses of the program, and indicate the relevance to you of the topics being presented.

The ITC also recognizes the outstanding panel session for ITC 2001. The program committee based solely on the session rating cards selected this award. The award is presented to:

**Searching for Common Ground Between Low-Cost and High-Performance ATE Systems**

*A. Kinra – Texas Instruments (Organizer),
B. Bennetts – Bennetts Associates (Moderator)*

The “top ten” papers (other than those listed above) selected by the 2001 ITC attendees on the session rating cards are: (listed in order of presentation at the conference).

**Frequency Detection – Based Boundary-Scan Testing of AC Coupled Net**

*Y. Kim, B. Lai, K. Parker, J. Rearick – Agilent Technologies*

**Testing Gigabit Multilane SerDes Interfaces with Passive Jitter Injection Filters**

*B. Laquai – Agilent Technologies, Y. Cai – Agere Systems*

**A Practical Built-in Current Sensor for $I_{DDQ}$ Testing**

*H. Kim, D. M. H. Walker – Texas A&M University, D. Colby – Texas Instruments*

**Testing Beyond EPA: TDF Methodology Solutions Matrix**

*S. Jain, G. Chema – Intel Corporation*

**Testing and Programming Flash Memories on Assemblies During High-Volume Production**

*F. de Jong, A. Biewenga, D. van Geest, T. Waayers – Philips Research*

**99% AC Test Coverage Using Only LBIST on the 1-GHz IBM S/390 zSeries 900 Microprocessor**

*M. Kusko, B. Robbins, T. Koprowski, W. Huott – IBM*

**OPMISR: The Foundation for Compressed ATPG Vectors**

*C. Barnhart, V. Brunkhorst, F. Distler, O. Farnsworth, B. Keller, B. Koenemann – IBM Microelectronics*

**Bitline Contacts in High-Density SRAMS: Design for Testability and Stressability**

*H. Pilo, R. D. Adams, R. Busch, E. Nelson, G. Rudgers – IBM Microelectronics*

**Testability Implications in Low-cost Integrated Radio Transceivers: A Bluetooth Case Study**

*S. Ozev, A. Oraloglu – UC San Diego, C. Olgaard – LitePoint Corporation*

**Unit Level Predicted Yield: A Method of Identifying High Defect Density Die at Wafer Sort**

*R. Miller, W. Riordan – Intel Corporation*