The DFT Cost Dilemma

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Today, it seems, lots and lots of designs use Scan, while not nearly so many use logic BIST. When does it make economic sense to use logic BIST?

When you can leverage BIST at the system level, the use of BIST is a no brainer. Enlightened system test architects beg for BIST to make their jobs easier. The benefits of more rapid and accurate diagnosis of hardware failures, of bringing a mission critical system up more quickly, and of perhaps catching defective ICs before the customer even sees a failure, overwhelm all other factors.

However, not every company is in a position to benefit from better system testability. Why would John Q. ASIC want BIST?

Not for fault coverage. ATPG does at least as well. Sure, you can run BIST at-speed, but you can generate transition tests also.

Not for design simplicity. Scan logic is a subset of BIST logic. Though the area impact of this logic is negligible today, it is still more to verify, to route, and to close timing on.

Not to make you sleep better at night. A small error in scan implementation can be masked out, with probably a very minor impact on fault coverage. A small error in BIST implementation kills your signature, and it is time to reduce your BIST clock speed, fall back on ATPG, or, at worst, respin.

So why would John Q. ASIC want BIST again? One good answer is to reduce manufacturing test cost. Doing much of test generation on-chip should, it is claimed, allow you to use cheaper ATE, and thus reduce capital costs, leading to reduced test costs and reduced product costs.

The feasibility of a low cost DFT tester, and what one would look like, is the subject of a great deal of debate. Let’s assume that some genius has come up with a perfect design for one. That is when the DFT Dilemma begins.

I have an easy metric to tell when BIST saves me money - whenever some ASIC vendor offers a discount for the use of BIST, I’ll know that BIST is a win, even when it won’t be used in a system. So far, I don’t know of anyone who’ll do that. Let’s look at why.

There are four players who are involved in a successful lower cost test strategy. There is the ATE manufacturer, who would have to invest in the development of a reduced cost tester in the hope that it would get bought. There is the ASIC manufacturer, who would have to buy the ATE, and dedicate at least one test line to BIST, hoping to fill up the line with BISTed ASICs. There is the customer, who would have to be convinced that they are getting a reduced price because of using BIST. (Neglect the system houses with other reasons to use it, the big market is in run of the mill ASIC designs.)

And, finally, there is the DFT tool maker.

Surprisingly, the DFT vendor is the least important piece of this puzzle. There appears to be enough demand for BIST tools to make them somewhat viable, and the BIST tool works the same no matter how and where the test is applied. DFT vendors have already done their job.

There are mutual dependencies among the other three. The ATE maker won’t invest in the low cost ATE unless the IC manufacturer is willing to buy, the IC manufacturer won’t buy unless he has customers who can fill up test capacity on the ATE, and the customer won’t commit to using BIST unless he can be offered a lower test cost, something possible only if there is a lower cost tester.

What makes things worse is the latency. Say it would take two years to develop a low cost ATE. It would take at least six months to get a new test flow up and running. This is not going to fit with ASIC development schedules, for any design begun today will be complete and shipped long before the low cost test facility becomes available.

What’s the answer? I don’t know. Even for scan, only the biggest vertically integrated companies use reduced cost testers. Until this problem gets solved, the potential of low cost test through DFT won’t be realized. So, although we use BIST for other reasons, if someone tells me it is going to save me money, I say “Show me the discount!”