ATPG versus Logic BIST - Now and in the Future

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The combination of full scan and ATPG have been utilized successfully by IBM for many years, and can now be considered ubiquitous throughout the semiconductor industry. Logic BIST has been around for a long time as well, but has only recently started to see wider adoption. Probably the largest hurdle to logic BIST implementation was the lack of availability of viable commercial tools. However, there are a number of vendors providing solutions and the tools are maturing rapidly.

Which is the right solution for your design? The simple answer is, it depends on the particulars of your design and test situation - How many gates, how many pins, the tester you’re planning to use, the frequency of operation, your experience with structured test techniques, and a number of other parameters. Until recently, scan seemed like it was always the right answer due to BIST overhead and a lack of tools. But the advent of large ASICs and other designs with one million or more digital gates has caused tester data volume, ATPG run time, and other problems that threaten the potential future use of scan.

However, BIST has its drawbacks, including complicating timing closure, additional area and routing overhead, tool complexity, fault coverage, power consumption, and other technical issues, not to mention the intellectual property royalties that several BIST vendors are demanding! So, for very large designs, it’s not clear that logic BIST is the only answer either.

Which technique will “win out” over the long haul is becoming harder to answer. It used to seem clear that for leading edge multi-million gate ASIC-like designs with frequencies in the hundreds of megahertz, some form of logic BIST, not necessarily STUMPS-based, was inevitable for at least two reasons:

- Tester data volume for full scan would simply grow larger than testers, especially legacy testers, can handle. Remember, old testers never die, they just keep going and going and going...

- We were heading towards a tester accuracy brick wall which would eventually obviate the possibility of successfully delivering test data from outside the chip.

Recent developments seem to cloud the crystal ball, though. An ATE vendor recently reported that highly accurate testers might be economically feasible, which could stretch the lifetime of stored pattern test [1]. ATPG and DFT vendors and universities are working hard on solutions to the scan data volume problem and making headway [2].

On the BIST side of the equation, there are a number of innovative ideas to address the issues of fault coverage, power consumption, timing closure (test point insertion), multi-frequency design, and other complicating factors, too numerous to cite here. Several of those solutions involve combining deterministic stored pattern tests with more conventional logic BIST, for example, the work of Das and Touba [3].

Perhaps these “combination” techniques are precursors of our future. It seems likely that no matter how ingenious become the methodologies of generating and applying stored deterministic and BIST tests, there will always be advantages and disadvantages of both approaches, and both will thus find a home in our test arsenal. That, to me, seems the most likely outcome. We’ll need to build more and more of the test function into the chip, but stored deterministic patterns will always be useful and probably necessary in some form.