Lowering the Cost of Test: ATPG vs. BIST

Cy Hay
Synopsys, Inc.

Today, full-scan design-for-test (DFT) in conjunction with combinational automatic test pattern generation (ATPG) is the most common and scalable way to achieve high manufacturing defect coverage. The methodologies and tools to support such flows are quite mature and are well accepted within the design community. However, built-in self test (BIST) continues to gain acceptance as an alternative approach for manufacturing test. As economic considerations become more important in choosing a test methodology, key arguments made for BIST are the minimal tester memory required to run such tests and easily testable IP cores. However, traditional ATPG approaches offer more design flexibility and usually deliver shorter test times and higher measured stuck-at fault coverage. Adding to the decision complexity, devices are often tested on large pin count, very high performance automatic test equipment (ATE), and this ultimately drives the cost of test. Neither of these techniques fundamentally require such sophisticated (and expensive!) ATE capabilities, but how can both ATPG and BIST be ultimately exploited to lower the ATE requirements, and thus the cost of test? And which methodology will emerge the winner?

The most important factor in this debate will be the emergence of low cost structural test (LCST) equipment. Once this class of equipment becomes commonplace on the manufacturing test floor, designers and test engineers will need to rethink and optimize their testing strategies to exploit the large potential in test cost savings. If these testers will cost less than a tenth of today’s full-featured ATE, is test application time still critical? Assuming that such testers will use commodity DRAMs, what happens to test data volume limitations? Will parametric, analog, and mixed-signal testing dominate the tester resources and time required to fully test the device? Will power consumption and dissipation during test emerge as a primary limitation? Any comparisons between ATPG and BIST should be made in the context of the LCST paradigm and should consider not only today’s test challenges, but future ones as well.

**Moderator:** Ron Leckie

**Panelists:** Ken Butler, Texas Instruments
Scott Davidson, Sun Microsystems
John Matthias, Agere
Peter Muhmenthaler, Infineon
Tom Williams, Synopsys
Yervant Zorian, LogicVision