AC-Scan: Microprocessors are ready …
But where is the Infrastructure?

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Position Paper

Very few design engineers would argue with the observation that modern microprocessors are designed to extract the last ounce of performance out of today’s manufacturing technology and as a result, more paths are likely to be critical and hence more likely to fail due to delay defects. The need to test for delay faults cannot be overemphasized.

Functional vectors have been used by many in the industry to apply tests at-speed with the hope of targeting delay faults. However, there are many barriers to the widespread adoption of functional test vectors as the mainstream mechanism to target delay faults. First and foremost, functional vector generation is a largely manual effort and the costs of generating functional tests for stuck-at faults, leave alone delay defects, are prohibitively high. Second, unlike the predictability offered by scan test vectors, functional test coverage is highly unpredictable. Third, in a high-volume manufacturing environment where test time and volume is paramount, functional vectors may not offer the same time and space efficiency as scan vectors. Fourth, fault grading functional vectors for delay faults (even for stuck faults) is generally a gargantuan task.

So, all of the above would suggest the adoption of scan to guarantee high fault coverage for delay faults. Scan has proven to be a time-tested approach to achieve high fault coverage for stuck faults. So, would it be possible to translate the success achieved in the stuck fault domain to the delay fault domain? Are we there yet?

The answer is: we are almost there. Scan tests have the potential to be the primary test mechanism for delay defects but we have to do some work before we get there. Many issues related to delay test infrastructure such as on-chip DFT hardware, testers, test metrics and test generation tools have to be addressed before we can say with any degree of confidence that scan tests can replace functional tests.

Consider the fact that implementing full-scan on performance/area sensitive hyper-pipelines is getting more and more difficult. Scan delay tests require implementation of special clocking mechanisms to ensure that the on-chip timing can be controlled accurately which places additional burden on the designers over and above the stuck fault DFT requirements. On-chip clocking is required since it is generally not feasible to control the pin timing accurately from low-cost testers. A scan test environment may also not quite mimic what goes on functionally for multi-GHZ chips. On the delay test metrics front, there seems to be little agreement as to what would be a good delay test coverage figure. Transition fault coverage figures are quoted routinely but one should remember that transition fault coverage quantifies only the coverage for gross delay faults. Transition fault coverage is a good start, but may not be enough. One should also remember that many ATPG tools today generate transition tests through the shortest observation paths. Path delay fault coverage may be more accurate: however, it is impractical to generate tests for all possible paths. This forces one to consider path selection criteria. However, do paths selected based on static timing analysis accurately correlate with the paths in fabricated silicon? Due to the tendency of microprocessor designs to stretch design and process constraints to the extreme, certain non-traditional delay fault models to account for failures due to circuit marginalities, cross-coupling/cross-talk etc. may need to be included. Design Automation tools will also need non-trivial improvement since the generation of delay tests of any kind (including transition tests) takes a heavy toll on ATPG efficiency. The above is just a short list of issues one may have to consider in any effort directed towards enabling scan-based delay tests.

In summary, scan delay tests have the potential to replace function tests but lots of work needs to be done on the design, coverage metrics and tools front before scan-based delay tests become a reality.