AC-Scan: Microprocessors are ready
But Where is the Infrastructure?

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Panel Synopsis

Over the years, scan design methodology has allowed us to tame stuck-at fault testing. Can scan do the same with delay defects? Our manufacturing process (deep sub-micron) and our chips appear (or intend) to be ready. But where is the infrastructure? Do we know how to analyze delay defects … or even agree on how to quantify and measure delay defects?

Some have even questioned if scan methodology is suitable for detecting AC defects. Here are a couple of extreme viewpoints:

**Scan and High-Speed defects simply don’t go together**
Scan has long been associated with slow-speed operation or low-speed designs. Using scan for detecting at-speed defects for 300 MHz + designs – speeds that are typical of microprocessors - will not work in practice. Shifting fast will create excessive noise and require more power than the package can handle. Shifting slow creates the problem of correctly switching to at-speed clocks between shifts. The power grid of a large design may not be able to handle the excessive current drawn for a few at-speed functional clock cycles. Then there is the problem of scan putting the design in non-functional states – that can possibly expose non-functional paths (or false paths) to the ATPG tool. Should we be throwing chips that fail non-functional paths? Leave scan where it belongs – stuck at the stuck-at faults. Focus energies on developing an automated functional test pattern generation and validation environment.

**AC-scan needs to, and will, get rid of ever-expensive functional testing**
The gap between testers and chip frequencies is widening by the day. Functional test solutions for 1G data rates are extremely expensive and driving up product costs. The Moore’s Law driven semiconductor industry of ours is holding back 2.5GHz designs due to cost-of-test concerns. Scan is the only viable way to address high-speed testability in a comprehensive way. AC-scan will build on DC-scan and chip industry will return to happy times.

The panel session, with your help, will attempt to find out who is right. Learn and share your views on where we all might be headed with AC scan.

**Moderator:** M. Ray Mercer, Texas A&M University
**Panelists:**
- Greg Aldrich, Mentor Graphics Corp.
- Rajesh Galivanche, Intel Corp.
- Kevin McCauley, IBM Corp.
- Amit Majumdar, Sun Microsystems
- Raj Raina, Motorola, Inc.