The SIP Alternative

ITC System-in-a-package Panel - Position Paper
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The stampede to System on Chip (SOC) implementation of electronic systems is being tempered by a fresh look at System In a Package (SIP) technologies as electronic systems developers struggle to incorporate more and more functionality into ever smaller products.

**Intellectual Property (IP)**
IP modules present thorny problems on technical, business and legal fronts. Verification problems for the IP modules require sophisticated engineering resources to ensure correct functionality in each application. Resources are required to insure that a rigorous design for reuse methodology was followed. SOC fabricators are struggling with similar issues that are addressed by KGD processes. Suppliers of die products have demonstrated effective test methods and reliability screens enabling user confidence in the quality and reliability of bare die - however, the unknown status of much of the IP today can delay entry of a new product into a time-critical market window.

**Functional Integration**
IC manufacturers are eager to incorporate more and more functionality onto a single chip, until the yield of the device becomes too low, or the cost of integrating dissimilar technologies becomes too high. Integrating similar technologies offers the best chance of success for a SOC application. All-digital modules, with the excellent design representation of Hardware Description Languages and associated verification models offer the simplest path for integration into a single chip solution. However, design for reuse, testability issues and signal integrity problems may well result in delayed introduction for the chip, leading to negative time to market implications.

The situation becomes even more problematic, however, when dissimilar technologies are being integrated. In developing a functional module that includes rf, flash or analog along with the logic, a close consideration of processing costs, module yields and testability will often point to the SIP solution as the cost-effective path. The cost-effective SIP assembly methods will take advantage of the compatibility of today’s SMT assembly technology with flip-chip-like devices, whether bare die flip chips or some form of wafer-level packaged devices which employ SMT mounting technology.

**Time to Market**
As time to market pressures continue to mount, a SIP can offer the advantage of “off the shelf” solutions to new problems. By integrating several ICs that have production history into a new products short-circuits the lengthy design and verification phase of SOC production. In addition, the IC supplier may consider making the IP available to customers after a successful SIP product introduction to allow a smooth transition to a SOC solution.

**Summary**
System in a Package offers the designer significant benefits in time to market, mixed technology integration, and lower costs. Improvements in KGD testing, die handling and assembly technologies and high density PWBs availability makes SIP a realistic option for OEMs. A significant challenge to implementing this technology is to insure that low-cost test technology is available for testing and reliability verification of SIP modules.