A System-in-a-Package (SiP) and its components can be tested at package, wafer, and substrate. Since the presence of a bad chip in the SiP at package test will cause the other chips and substrate to be discarded, or require a repair that would be too expensive for a consumer product, it is imperative that the chips be known to be of high quality before they are assembled. This requires that all chip tests and reliability screens be performed at wafer probe or, less economically, on bare, discrete dice. This in turn requires automatic test equipment (ATE) that is capable of performing full performance, at-speed probing and wafer-level reliability screening.

At-speed probing is difficult because rapidly increasing product speeds keep exceeding more slowly evolving probe and tester interface technology. Economical reliability screening perhaps is a bigger challenge. Though many effective known-good die (KGD) schemes have been developed for industrial and aerospace multi-chip modules (MCM), most involve burning-in discrete, bare dice in special carriers or temporary packages, methods that are too expensive for consumer electronics. Low cost dictates screening in wafer form and in a short time.

Wafer-level burn-in systems have been introduced recently but they challenge contacting technology while burn-in takes a long time. Other, faster screens that can be performed on standard or simplified ATE are under intensive study but, so far, no combination of stresses and detections has been found that is as effective as burn-in without a high fraction of false rejections. Some of these methods are limited by ATE, e.g. IDQ signatures by device power supply current measurement resolution and speed, while others are limited by decision criteria, e.g. how low an operating voltage in a Low Voltage Test (LVT) indicates a defect.

Since a consumer SiP is composed of only a few inexpensive chips on an inexpensive substrate and goes into an application that demands less reliability, its chips are not required to have the yield and reliability of traditional MCM KGD. Consumer SiP chips only need to be good enough to minimize the manufacturing and warranty costs as determined by modeling the cost of the product in the technology chosen to build it.

Likewise, SiP requires good enough substrates. Substrates, both interconnect-only and with embedded passive components, can be economically tested with techniques that have been highly developed for printed circuit boards. The new challenges for SiP are finer (though fewer) conductors and smaller passive values. Simple substrates made in a high yield process can skip test.

SiP simplifies some aspects of test. Since the major reason for implementing a system in a package is to partition the system’s functions among chips and substrates built with the most suitable device and process technologies, each die can be tested with equipment that is tailored to its function and technology. This is most economically done with function-specific testers built off a common platform.

Package (final) test is simpler since the dice and substrate have already been tested and do not need to be reverified. Final test only needs to verify the placement, interconnection, and possibly the interaction of the SiP’s components. Placement and, to some extent, interconnection can be verified by non-electrical methods like automatic optical and X-ray inspection. Digital chip-to-chip connections can be verified electrically by boundary scan but a comparable electrical method does not exist for analog and RF connections. When the chips’ or substrate’s manufacturing tolerances are large enough to cause significant variations in the product’s performance, the package test must also verify the circuit’s performance. In this case an SiP would look the same to a tester as an SoC so it would be functionally tested on an SoC tester.

Therefore, the biggest difference between test of an SiP and test of an individually-packaged chip (an SoC) is that SiP emphasizes wafer test.