System-in-Package is Coming to Consumer Products: Is Test Ready?

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Introduction
System-in-Package (SiP) refers to a design and manufacturing style where multiple semiconductor dice and passive components are interconnected on a common substrate with fine pitch wiring and are encapsulated by a common enclosure. Figure 1 shows a cross-section of one possible implementation of a SiP device.

SiP enables integration of heterogeneous technologies like RF, memory, analog and passives (RLC) into one package, which otherwise is very difficult, if not impossible, to do on a single die. This property of SiP has allowed it to become a viable and accepted complement to system-on-a-chip (SoC) in reducing physical volume, weight, and power consumption; characteristics that are especially valuable for portable, personal electronics. Examples of these products are cellular telephones, personal digital assistants, music players, global positioning systems, digital cameras, and combinations thereof. The fact, that portable personal electronics is one of the fastest growing markets, draws the industry’s attention to any problems in its way.

Issues
While the ability of integrating a mix of technology is helpful in creating portable electronics, it brings its own set of test challenges. For example testing of embedded RF and passives (RLC), which may impact design as well as the equipment that will be used to test them. These challenges become even more severe when the limited access to the components within a SiP and the cost constraints of consumer devices are taken into account. This panel will try to identify such test issues and possible approaches to tackle them. The key questions that the panel will address are:

• What part of SiP testing can be leveraged from SoC, PC boards, MCM?
• What test problems and opportunities are unique to SiP?
• How good does a “Known Good Die” (KGD) need to be? Is a “pretty good die” sufficient?
• How can analog and RF components be tested with limited external access e.g. can a radio be boundary scanned?
• How is a substrate with embedded passives tested?
• Do we need to change standards like IEEE 1149? New standards?
• How should test be distributed through the process of building a SiP? How should this be determined?

Panelists
Moderator: David Keezer, Georgia Tech
Panelists: Paul Roddy, Motorola Inc.
Lee Whetsel, Texas Instruments
Peter O’Neill, Agilent Laboratories
Larry Gilg, Die Product Consortium

Organizer: Ajay Khoche
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