The proliferation of complex SOC’s with heterogeneous functions such as Logic, DRAM, Analog, Flash and FPGA on a single chip and/or package is driving the need for fundamental changes in the approach to Test and DFT. Different than the past 25 years of silicon integration, where we have largely been dealing with increasing complexity of similar function, predominantly Logic and embedded SRAM, the new classes of SOC’s present new and unique technical and economic challenges. While historically the focus and importance placed on DFT has varied greatly across the industry, with these new types of SOC’s, DFT will be a make or break proposition for market success.

The fundamental challenges of time to market, test cost, yield and quality are the same ones we have always faced. However, traditional approaches to DFT and Test are not going to be successful in the future. The interdependency between Design, EDA and Test Engineering is going to be stronger than ever and comprehensive technical and economic analysis of the DFT and Test Strategy as part of the whole design process are going to be of paramount importance. The problems presented by complex SOC’s cannot be left for the ATE companies and Test Engineers to solve. The onus is on the Design community, in collaboration with EDA tool developers and Test Engineers to develop the design tools and methods that will enable cost effective manufacturing test, as well as diagnostics and other debug/bringup capabilities necessary to develop and launch SOC products in a timely manner. If the right choices are not made at the design level, it will be largely impossible to achieve acceptable test coverage and affordable test costs.

It is more likely that the economic challenges of SOC testing are going to outweigh the technical. There are various test approaches available today including “SOC Testers” and multi-pass testing which can be used to test these complex devices and achieve acceptable quality levels assuming some reasonable level of DFT is employed. However, in many cases, because of conflicting test methodologies and requirements, the test cost for an SOC will greatly exceed the sum of the test cost for standalone components making up the SOC function. This will be true even in cases where a lot of focus has been placed on DFT by the design team.

The dilemma is that SOC test costs, because of these conflicts, are not scaling at the same rate as the cost per transistor. The implications of this are escalation of test cost as a percentage of total packaged die cost, at a minimum, and test cost as an economic barrier to successful SOC implementation, at the extreme.

Lastly, not to ignore the role of ATE companies, the availability of very low cost DFT Testers, capable of parallel testing up to 8 devices or more, are the strategic leverage point as opposed to the higher cost SOC Testers that are the primary focus today.

In conclusion, the winners and losers in the world of complex, heterogeneous SOC’s will be determined by how well the Design, EDA, Test and ATE communities collaborate to develop an integrated Test solution that meets the technical and economic objectives of the marketplace.