Changing Economics of SoC Testing: Who Owns the Market?

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System-on-a-chip (SOC) designs are gaining popularity, yet the complexity of these designs can slow down product development and increase cost rather than speed things up. The new economy, the raising role of SoCs and their escalating costs are forcing the electronic industry to re-examine the existing approach of design and test. For innovative products the integrated SOC development environment promises to provide the greatest productivity increases, and therefore the fastest time-to-market while keeping costs under control. Integrated development environment means not only thinking how to approach physical design, but for industry, including customers and vendors, a fundamental shift is required in making all critical decisions during system specification and high level design. What the integrated SOC development environment should look like? What are its essential components? The list of decisions is ranging from platform choice, to software-hardware partitioning to IP selection to packaging etc. The list is long but higher level each decision will be made better outcome will be generated and better trade-off can be reached. Here, our main focus is on testability. Testability meaning low level SCAN insertion issues, overall SOC test methodology and ATE selection. Today, there is a believe that design-for-test (DFT) technology and tools will help in solving increasingly high complexity and cost of SOC testing. DFT including build-in self-test (BIST) gains acceptance and change the development environment. With a decision on a DFT strategy for SOC the required set of software tools and ATE are completely different. The software support for DFT becomes comprehensive. The requirements for ATE change and can vary in level of cost, complexity and software integration. Several ATE vendors are researching and introducing a new class of structural testers, often called DFT testers. EDA companies are facing the same dilemma from software point of view.

The goal of this panel is to discuss the changing market of SOC testing and to identify a potentially winning strategy.

Moderator: Bozena Kaminska, Fluence Technology
Panelists:
   Roger W. Blethen, LTX Corporation
   Glyn Devies, Credence Systems Corporation
   Jim Hogan, Cadence Design Systems
   John Harris, IBM Microelectronics
   Thomas Newson, Agilent Technologies
   Lori Watrous-deVersterre, Mentor Graphics