THE FUTURE OF HIGH END ATE

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Today’s challenges

The reality of TODAYs semiconductor manufacturing business is delivering the right solution to market, on time, and with minimum cost. Today’s silicon integration levels are enabling system on a chip to become a reality. The SOC market is characterized by the explosive internet market and communication market, the rate of change is extreme along with a critical pressure on cost. The net is that our customers deal with a huge amount of uncertainty as to what is going to be the next "high flyer", the volume driver, for manufacturing.

So the questions of the manufacturing community are:

• How can we minimize the overall cost envelope?
• Can we ramp up fast enough?
• Can we manufacture today’s and future technologies?
• How can we maximize utilization?

Agilent responds to this challenge with a single scalable platform TODAY, allowing to use fully compatible systems across the floor, to maximize flexibility and utilization.

Is this picture going to change?

Yes, we are seeing already today that the gap between what is required during the characterization phase and what is being required in a matured manufacturing phase is growing. We see structured test approaches being deployed leading to "intelligent" manufacturing flows targeting the different sockets at test at the main sources for manufacturing defects of that particular step. We see multisite test (parallel test of multiple devices) as well as concurrent test (testing independent building blocks on one chip in “parallel”) as fundamental to drive down cost of test.

This approach truely redefines the role of high end ATE to be the characterization platform and the gating unit in the final test step which is being complemented by DFT focussed test steps. But is the same thinking applicable in the high mix, high change over, fast change, cost driven SOC world, especially mixed signal SOC?

The answer is most likely: Over time.

One of the key gating items in this process are analog properties. Tools for Design for Testability /structured approaches in the analog world are lagging behind, process defects/designs flaws in this area still create substantial amount of risk requiring parametric validation. At this point in time our customers value the option use truely compatible flavours of the exact same platform to move quickly from engineering to manufacturing.

So we see the high end ATE systems continue to exist, with a different twist though: With built in scalability to very low capital outlay, with modularity to add capability on a as needed basis.