Big-Iron Testers are a Reality – Their Requirements and Role

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Conventional “big iron” testers are a standard tool in most, if not all, integrated circuit manufacturing test flows. This is expected to continue. However, as circuit attributes, such as architecture, performance, density, size, pin-out and parametrics change over time, associated test and test execution challenges are also periodically redefined. Because of this, determining the role and capabilities of the next generation tester is a major activity of the semiconductor and measurement industries.

The value of re-engineering a conventional tester becomes apparent in the example of system-on-chip (SOC) testing. From a test point of view, SOC’s can be thought of as multiple chips all packaged together because they contain very different categories of embedded cores (e.g. analog, RF, high/low speed digital, etc.) each requiring a very different type of test. Rather than complicate the test flow with a number of independent standard test equipment, another possible solution is to use a single test-head with pin electronics bundled to perform functions dedicated to test a particular circuit (or core) type. By echoing the need of the circuit, the result is more parallelism and a better managed test flow (i.e. fewer test insertions). The choice of strategy is, of course, dependent on the resulting cost of doing the test but it is clear that there is a potential for a re-architected tester to positively influence test execution expense.

Testers are expensive, very specialized, low-volume equipment. In an effort to reduce test execution expense, one recent thought is to complement the test flow with lower-cost “structural testers” which exploit on-chip design for test. Typically, however, these equipment can achieve only a limited test coverage the level of which depends on the capabilities of the structural tester which in turn capped by the extent of its “low-cost.” The success of the strategy depends on its use in the test flow but for most high density IC’s, inevitably, a higher-end tester is still needed to properly complete the manufacturing defect screen. The key is that until a robust and proven low-cost alternative (DFT or otherwise) exists, the higher-end testers will continue to quickly provide the test execution solutions necessary to the high paced design and production environment. After all, chips are being made now so their needs have to be satisfied now.

A panel industry experts will discuss why high-end testers remain a realistic and an essential part of the production flow. The focus is to identify the basic test needs addressed by these equipment and for which there is no economical alternative. Specifically, a number of questions can arise. For instance: Given the use of a structural tester, how can the complementary role of the high-end tester be defined? Can a high-end tester be made cheap enough such that a structural tester is not needed? Given the state of DFT technology, for which classes of chips is a flow dominated by higher-end testers required? What fraction of the semiconductor IC market does this represent? The panel will also attempt to project the change in capabilities of the conventional tester so that it competitively adapts to changing technology.

Moderator: Steve Sunter – LogicVision
Panelists:  Ken Mandl - Teradyne
           Kazuo Ito - Yokogawa Electric Corporation
           Terry Larson - Credence
           Ulrich Schoettmer – Agilent Technologies
Organizer: Fidel Muradali – Agilent Technologies