ITC 2000 Panel Discussion

What defects escape our tests ... and how will we detect them in the future?

Phil Nigh
IBM Microelectronics
nigh@us.ibm.com

Higher speeds (e.g., >1GHz) and smaller feature sizes are making ICs sensitive to new types of defects. Thus, VLSI testing must change to detect these new defect types.

In this panel, we will discuss these new types of defects and what tests must be added to the suite of tests to ensure they are detected.

Each panelist will show 1 or 2 types of defects that currently pass today’s production tests. They will describe how each defect behaved and why they could not be detected.

Finally, each panelist will discuss what new test methods must be added to their suite of tests in the next 5 years to ensure these defect types are detected. The “new” test methods that will be discussed include:

- very low temperature testing
- very low VDD testing
- high voltage stressing
- testing at burn-in conditions
- new approaches to IDDQ (IDDX) testing
- thermal testing, “depowering”, retention test for logic circuits
- delay-oriented structural testing
- logic built-in self test (BIST)
- embedded memory retention and BIST

Moderator: Phil Nigh, IBM

Panelists:
Anjali Kinra, Texas Instruments
Mike Rodgers, Intel
Peter Maxwell, Agilent
Ed McCluskey, Stanford University
Bill Huott, IBM