Enough Test with DFT-Focused Chip Testers

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Why do we need to introduce a new generation of testers for testing products with significant DFT features?

It seems mandatory that the test coverage has to be stabilized at least on the actual high level. While products are developing fast towards higher complexity and signal performance the constraints on ATE features get more aggressive. The required ATE accuracy is one important factor, see ITRS 1999 roadmap.

The traditional test approach assumes a product and a tester where the ATE takes the active part and the product offers maybe some passive testability features. Timing accuracy has to be provided by the ATE. In that sense test cost highly depends on the number of high performance digital ATE pins interfacing the assumed SoC products. The increasing amount of test data to be exchanged between ATE and DUT is another cost factor.

Without integrated test solutions where part of the test function is located on chip we have to deal with more expensive ATE. Such testers can hardly cope with the ongoing performance increase of the products. Higher specific test cost does not fit to mass markets demanding for low cost SoCs.

While built-in self-test can solve test data bandwidth and performance test issues at reasonable cost the requirements for ATE will change. Full speed digital test features can be reduced. Besides precise clocking such ATE may focus on DC measurement, accurate power supply, BIST control interface and support of multiple parallel test on wafer and package level. Such a basic tester, which is not dedicated to a specific SoC product, should be available at reasonable low cost.

Optimized analog test functions as a complement of the SoC’s mixed signal interface need to be provided as an extension by that new ATE generation. Due to the fact that there is no standard SoC the flexibility to setup various tester configurations is very important. A suitable approach would be a tester, which acts as a platform test controller for various types of dedicated resources. Only a basic set of test features would come with the platform. The product features determine how much dedicated test resources have to be added.

Most of the BIST solutions are good for go/nogo testing with poor support for fault analysis. Full-blown general-purpose testers as of today may serve that market. But how long? How to analyze GHz performance through MHz product pins? Advanced BIST techniques will enable to use probably the same low cost ATE for diagnosis purposes.

An extension of current scan based DFT solutions towards various kinds of digital Built-in Self-Test can solve the upcoming production test issues. High precision test of digital signals needs to be done on chip. Analog tests should be transformed into the digital domain wherever it is efficient.

With DFT solutions for high test coverage in place the functional testing through digital product pins can be excluded from standard manufacturing test. Then a DFT-focused chip tester provides enough test for the digital part of a complex SoC.

It is still open whether the “DFT-Tester” should serve as a single platform for multiple analog extensions to keep test floor logistics easy. Multiple parallel testing on wafer and package level supported by such dedicated ATE serves the digital domain probably very well.

There seems to be no alternative to DFT-focused ATE, if we want to cut test cost by one magnitude or more.