DFT-Focused Chip Testers – What Can They Do?

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DFT-focused or structured testers are becoming the latest thrusts in the ATE industry. They represent a major departure from the last thrust towards SOC testers. An SOC tester is a test engineer’s dream—high performance digital test capability with lots of pattern memory, racks of mixed signal tools, and at least some token memory test capability thrown in for good measure. So who wants a DFT-focused tester that’s probably simple enough to be built in someone’s garage?

The primary feature of DFT-focused testers is that they are not capable of running high-speed functional vectors. Most of the cost of a high performance digital tester comes from the high-speed, highly accurate pin electronics and the pattern memory required to maintain high data rates. The promise of DFT methods like full scan and BIST is to eliminate the need for traditional functional test vectors. Eliminating this requirement allows DFT-focused testers to be relatively cheap, which is why they are becoming popular.

The first question asked when evaluating DFT-focused testers is ‘What can they do?’ From a traditional point of view, many test engineers will probably answer ‘not much.’ A DFT-focused tester typically can’t do some of the things test engineers spend the most time on today, like characterizing speed paths in a high performance device. A DFT-focused tester can’t even directly verify data sheet AC timing parameters. So what can they really do?

By definition, DFT-focused testers need to be defined based on the DFT techniques on which they are focused. A cheap DFT-focused tester with one high speed clock can’t do much if the devices it needs to test require two accurate clocks for delay fault measurements. A DFT-focused tester which supports 128Mb of scan at 50Mhz will include needless expense if the devices it needs to test use BIST with minimal scan access.

Obviously, the key to successful implementation of a DFT-focused tester strategy is the DFT, not the tester. DFT-focused testers need to be designed to match the capabilities of the DFT techniques used in the devices that they will test.