DFT-Focused Chip Testers: What Can They Really Do?

Gordon D Robinson
Credence Systems Corporation, Fremont CA

The 1999 International Technology Roadmap for Semiconductors included a section describing testers focused on designs whose test strategies are dominated by DFT and BIST. The forecasts of $20M testers for full-feature functional strategies and “approaching only $200/pin” for DFT-focused testers has both exposed a fundamental cost problem, and outlined a potential solution.

DFT techniques have been used for many years to ensure high coverage, automate test generation, to help debug and so reduce time to market. A few companies have also developed low cost test equipment similar to that forecast by the ITRS.

The reactions to the ITRS predictions are highly varied: almost everyone would love to have much lower cost test equipment; but nobody wants to put the quality of their product at risk. And some are concerned that such equipment is too low cost for building it to be a viable business.

This panel session brings together the different viewpoints on such testers: those who have developed and used very low cost testers, the ATE industry, and the semiconductor manufacturers who want to get test cost benefits from their DFT investments.

Those who have already implemented DFT-focused testers will show the different approaches they have taken, lessons they learned about the difficult issues in the design and adoption of this equipment, and changes that were needed in DFT technology and tools to make these systems succeed.

The ATE industry sees DFT-focused testers as both a threat and an opportunity. A threat to the high-priced full-featured tester business they are used to, and an opportunity for additional business for some companies.

The semiconductor companies that hope to adopt DFT-focused low-cost testers know that something has to change to enable the savings. They will address the types of change they anticipate making, the test strategies they expect to use for wafer, package and other tests, and why they are confident that their product quality will not be harmed.

We expect that all participants, and the audience with their questions and experience, will learn from each other what such testers can do, and how they can become reality.

Organizer: Gordon Robinson, Credence
Moderator: Tony Ambler, UT
Panellists: Marc Loranger, Credence
           Al Crouch, Motorola
           Don Wheater, IBM
           Peter Muhmenthaler, Infineon
           Steve Comen, Texas Instruments