It’s their problem – Not mine!

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Electrical noise is like an inherited disease. Its effect can be minimized through the right medicine and procedures, but it can’t be eliminated. It has been a fact of life. Renewed interest in noise is because we’re just recently seeing more designs having failures due to an electrical noise effect.

It’s not new

It really isn’t a new problem; it’s just that there are more designs becoming susceptible to the electrical noise. This susceptibility has increased with each shrink of silicon technology, which has reduced operating voltages consequently decreasing a gate’s noise-margin. Technology shrinks increase inter-signal coupling, which has made coupled noise voltages higher. Additionally, interconnect resistance has skyrocketed accentuating the effect of resistance-isolated coupling noise.

Designers using dynamic circuits have had to cope with the presence of noise for more than 20 years, and have learned how to analyze its affect on the design.

Electrical noise was a circuit issue in the 1980’s when circuits may not have had the correct logical value due to some aggressor signal transitioning. About the mid-1990’s, that same noise had also been seen causing significant slowing up or speeding down of critical circuit paths.

All aspects of the design are hit

Two fundamental design concerns with electrical noise are its affect on a design’s reliability and performance. Reliability is a concern when this noise causes a nasty NPN parasitic transistor issue like CMOS latch-up condition or dynamic node problem, causes a signal to have the wrong perceived logical value, or to speed up a signal such that it causes a data-clock race condition. Noise affects performance of a design by slowing down critical circuit paths. Both the slowing-down and speeding-up of circuits could result in a design’s incorrect logical behavior.

The overall effect of electrical noise hits all aspects of design. It’s a problem at both the architecture and floor-planning design stages as it influences and causes a widening of the min/max global signaling delays, thus creating more uncertainty of the timing for those signals.

Electrical noise has to be analyzed and compensated for during a design’s implementation, and this is taking more designer time for each process generation. Even clock distribution is affected when you correctly analyze previous cycle electrical noise to the next cycle’s clock edge. This directly attacks the idealistic dream of having same-time arrival clocks across the design, making the design of clocking much more difficult.

Furthermore, manufacturing test is affected by this noise, as it becomes a very important part rejection or selection criterion.

It’s bounded (on paper)

Designers armed with circuit analysis techniques can achieve a reasonable bound on most electrical effects. Bounding of electrical noise can be of absolute worse-case or using one of many statistical methods. Bounding methods make assumptions between the relationships of aggressor-noise to the victim’s signal integrity requirements. For most cases, this bounded analysis is quite adequate and allows the designer to make quick assessment of possible circuit problems. For instance, accumulative aggressor-noise can have strong influence on critical-path delay. By bounding that coupling-induced delay during analysis, the designer quickly knows the possible minimum and maximum arrival times without having to be concerned with how the accumulative noise was estimated. As a result, the designer knows which circuit paths probably set the design’s operating frequency.

Unfortunately, the same designer identified critical-path in a real chip has to be tested – ah, real life! An actual silicon part is neither worse-case or statistical, it’s real. So, the assumptions made during analysis have to be reproduced in test for that part. This means maximizing the delay of a logic-path by simultaneously inducing the worse accumulated slow-down via coupling along the circuit’s path. This is very hard to accomplish, and in reality, may disagree with the pre-silicon analysis information.

Overall, noise affects everyone in the product design cycle. Whose problem? – as everyone would like to say, “not mine!”