Internal CAD + EDA + Services = turmoil, fencing or bliss

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Abstract
Because using EDA tools are "business as usual", best practices, challenges, successes and painful experiences in integrating EDA tools/services into an established design flow is the subject of this panel. Usage conflicts do exist among all parties. The goal is to identify the best path to success.

Integrated circuit design has moved far away from bread-boards and hand-drawn rectangles. Accommodating modern process technology, circuit sizes and production volume, force the need for automation of design tasks and complex rapid CAD analysis.

Today, EDA tools are an essential part of "business as usual." Many design automation solutions solve a well defined problem which can be carved out of a design flow. Because of this, these tools operate best as stand-alone "point solutions." Of course, since chips are built, this approach works. But at what cost? Treating the targeted design issue as if it exists in a bubble can create complications since the proposed EDA tool must eventually be integrated into an end user's established flow or more encompassing methodology. Odds are that the EDA tool developer or the external consultant is not as well acquainted with the user's flow or chips. This is often overlooked and can incur time and effort at the expense of the user. Indeed this hidden cost can become expensive.

Regardless of the reason, the chip producer shoulders the brunt of any failure to deliver. Thus, the ability and ease of including a point EDA solution into a non-homogenous design flow is important. In fact, because any cumbersome procedure affects productivity, even for the sharpest of ideas, the final usability of a tool or technique can make or break its acceptance. Depending on tool and concept maturity, a solution rarely works “out of the box.” From the perspective of creating a chip, the situation is influenced by factors such as, adaptability to the user’s design and test methodology, the possible use of external services, and interfacing embedded cores from external vendors (or even different design teams over time). It can also be argued that while some techniques are now well ingrained into the science (e.g. ATPG and Scan), every 1.5 years the challenges posed by changes in fabrication technologies and design requirements scream for the development and re-development of new tool solutions at a pace which can create the impression of tool sets never stabilizing. Nevertheless, it is in the best interest of the EDA provider and user that the produced solutions work as smoothly as possible.

The industry is poised for another paradigm shift in design technology. The current situation is one in which a number of different in-house or external EDA solutions are blended together into a design flow. The next step is to tailor the flow to a particular chip category (e.g.SOC with reuse, SOC with analog, with RF, flat, etc) or design style (e.g. in-house, embedded cores, hierarchy, etc.). Before we can move forward, the basic components - the CAD techniques within the flow, designers, 3rd party services, and all the players from customers to the test floor to silicon debug must smoothly interface. This panel touches only on the tip of the iceberg - the currently faced hurdles between EDA and customer designers.