Designs are Changing – Can Test Keep Up?

Robert C. Aitken
ASIC Design Methodology
Program Manager
Agilent Technologies

The ongoing challenge of test is to obtain high quality at a reasonable cost. Increasing design complexity, signal integrity, and power issues mean that design-for-testability can no longer be treated as an add-on. Similarly, serious attention is needed for parametric testing or the cost requirements for GHz-frequency test will be prohibitive. Is the industry ready for the challenge?

Design issues
Historically, cell-based ASIC design has proceeded in a linear fashion from synthesis to cell placement to routing to timing extraction to artwork verification. The linear nature of the design process meant that the steps were largely independent of one another. As a result, any individual step could use a unique tool, and there was no need for a single vendor to supply the entire tool chain. Design-for-testability could remain independent of the rest of the design process.

As design moves into so-called deep-submicron processes (below 0.18µm), the design process is changing. As processes shrink, the delay associated with wiring is increasing as a percentage of overall delay. In addition, effects that were previously ignored such as power dissipation, signal coupling and IR drop are routinely breaking IC designs. As a result, it is no longer possible to design the logic and wires independently, and new design tools are being proposed. These tools merge formerly standalone steps in the design flow, and, as a result, standalone DFT tools may find themselves without a place to interact in the design flow. In addition, customized DFT structures must be explicitly incorporated into the entire design flow, and not added separately or as afterthoughts. DFT engineers must not be guilty of throwing their circuitry “over the wall” to IC designers!

Timing
In some applications, such as networking, device I/O speeds have already surpassed the ability of testers to measure them. “Conventional” functional test cannot work in these areas. Some other measurements will need to be made instead to test device I/O, and their results correlated to device timing failures. Timing test problems also exist inside circuits. Possible solutions include built-in loopback tests, at-speed scan testing, path-delay testing, low-voltage testing, and parametric measurements (e.g., dynamic current, energy consumption, current ratios, etc.), but strong experimental evidence correlating these to functional failures is needed. Failure to test delays at chip test means increasing expense in board and system test later on to identify both defects and design margin problems resulting from inadequate characterization.

Faults
Some major differences stand out between CMOS processes of the 1-µm generation and today’s: First, the current generation has more levels of metal (6 versus 2). Second, the metal lines themselves are relatively thicker (their aspect ratio has changed), and flatter. Finally, the transistors themselves have smaller geometries and are thus subject to “deep-submicron” effects. The additional metal, and particularly the additional vias between layers mean that interconnect defects are more common (especially resistive defects), and that intralayer capacitive and inductive effects will be more common. Many of these are inadequately modeled during design and may manifest themselves as failures under some circumstances. The boundary between design validation and test fades under these circumstances. The complexity of modern processes means that fault models developed and validated for earlier technologies must be reassessed. It is unlikely that tests for stuck-at faults will disappear any time soon, but they need to be applied under the right conditions, augmented with parametric measurements, and validated for noise margin, power consumption, and so on.

Implications
In each case, conventional test tools will need to interact with the rest of the design methodology in a tightly coupled fashion. Whether checked after the fact or designed correct by construction, electrical signal integrity and power distribution issues will need to be tightly coupled with high-level synthesis, and DFT will need to interact with all of these and at all levels.