In a collaboration initiated in 1997, Fujitsu and Philips have jointly developed a Design-for-Test methodology to facilitate assembly interconnection testing of complex memory devices. Complex memories require an initialisation sequence or are accessed by a more complex protocol and therefore complicate assembly test – examples are SDRAM, FCRAM and Flash. With the trend towards smaller pin pitch and chip scale packages (CSP) for memories, testing of solder connections becomes ever more complicated and expensive.

Especially in the light of the extremely cost sensitive memory market it is a major challenge to develop fully comprehensive test diagnostics for efficient detection of static solder connection faults at a negligible cost impact allowing the user to use a simple low cost tester. These main design objectives led to the development of the boundary-scan compatible Static Component Interconnection Test Technology (SCITT). SCITT allows to significantly improve fault diagnosis and dramatically reduce test time resulting in savings on production cost that are greatly exceeding the additional cost for implementing the test circuitry in the memory device.

SCITT is based on a simple loop-back function incorporated in the I/O area of the memory device using XNOR logic to minimise the number of test patterns and maximise diagnosis resolution providing precise fault indications (device, pin and type of fault) at a 1000 fold reduced test time. The generic nature of this test technology makes it easily applicable for all memory densities and device organisations.

Fujitsu estimates the additional die size required for the implementation of the SCITT logic to be LESS THAN 1%. The performance impact as another critical parameter especially for high-speed memories is estimated to be LESS THAN 1%. SCITT does not require a pin-out/package change since it uses existing pins by multiplexing the test functions onto them – this approach allows a simple replacement of existing memories with SCITT enabled memories minimising cost and time-to-market. The first device from Fujitsu, the 3rd gen. 64M(x32) SDRAM with SCITT functionality is already available in mass production. The functionality of the SCITT circuit was successfully verified on this device and the design targets for die penalty and performance impact were fully achieved with 0.3% die size for the SCITT circuit and 50ps increased access time ($t_{AC,Ref}=6\text{ns}$).

Fujitsu plans to offer memory devices with the SCITT feature at prices that will allow customers to greatly reduce the total manufacturing/testing cost of their products. The need for board assembly test especially for high volume consumer electronics applications is very likely to further increase in the future and Fujitsu’s SCITT enabled memory devices offer a low cost and feasible solution to solve such testing issues providing a competitive advantage to our customers.