Benchmarking DAT with the ITC’99 ATPG Benchmarks

Mario Konijnenburg¹  Hans van der Linden  Jeroen Geuzebroek²
¹Electronic Design & Tools
Philips Research Laboratories
Eindhoven, The Netherlands
email: konijnen@natlab.research.philips.com
²Delft University of Technology
Faculty of Information Technology and Systems
Delft, The Netherlands
http://cardit.et.tudelft.nl/~linden/testing/test_frames.html

Introduction
In the framework of the new ITC’99 ATPG benchmark set, a short description is given of the Delft Advanced Test generation tool (DAT), because it has been used to test a number of the ITC’99 ATPG benchmarks. However, at the moment of writing no results are available for publication.

The Delft Advanced Test generation tool
Since 1992, DAT is being developed at the Delft University of Technology in the Netherlands. Currently, it can handle combinational (full-scan), partial scan, as well as full sequential circuits.

In combinational circuit mode, the tool supports the stuck-at fault, the Idq node toggling and bridging fault, and the gate delay fault model. Many techniques have been developed to improve the ATPG efficiency; this means reducing the number of aborted faults and the test set size, and not in the least ATPG CPU costs and memory consumption. Fast test generation is performed using an extended FAN algorithm combined with (parallel pattern) fast fault simulation techniques. To achieve compact test sets pre-identification of untestable faults is performed to improve the Compact Oriented DEcision Making (CODEM) in test generation. Bus-conflicts prevention is performed in various flavours. To tackle the hard-to-handle faults recursive learning techniques are applied.

In sequential circuit mode, the tool supports the stuck-at fault model. A sequential test generation system has been developed based on the combinational TPG algorithms. The forward time processing methodology during fault propagation and the reverse time processing methodology during state justification is applied to achieve maximum profit of the combinational circuit techniques. A 16K valued power-set logic is applied to increase signal value resolution and to improve the ATPG efficiency. (Il)legal state learning techniques are applied to constrain the TPG to legal states.

Currently Test Point Insertion (TPI) and Logic BIST techniques are being developed. We use DAT as engine for TPI techniques to improve the random testability of circuits for BIST and to reduce the test set size for ATPG.

Since 1995, DAT is the kernel of the Philips ATPG system AMSAL. An almost complete overview of the published techniques can be found in [1] and [2], except for TPI, logic BIST (Jeroen Geuzebroek), and gate-delay fault TPG and FS (Frank Pöhl of the University of Bremen, Germany).

The ITC’99 ATPG benchmarks
Currently, DAT performs well on most of the well-known ISCAS benchmarks. However, a case study on the Philips 80C51 for sequential ATPG showed, for example, that the sets do not reflect real designs (anymore); see paper 31.2. The ITCYY benchmark set provides a number of realistic present-day circuits; therefore, the set is a new challenge for test researchers. Nevertheless, addition of huge circuits (>1M nets) in the set would make the set even more valuable, because in our experience they often show the large time and memory complexity of current techniques.

References