Functional ATE CAN Meet the Challenges

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1 Introduction

The SIA roadmap presents some challenges which focus our attention on the cost and performance of functional ATE. High cost and demanding test performance requirements have been perceived as potential barriers to semiconductor production for the last 15 years or more - and predictions of the “death of ATE as we know it” have been heard at least that long. With forecasts of $35 million for 5300 pin testers frightening fab line managers worldwide, these predictions seem even more justified now. But are they?

2 The Performance Measurement Requirement Will Not Go Away

Traditionally, functional ATE has had several very different roles, including --
- Establish that the tested device operates within its specifications.
- Determine device operating margins and performance limits.
- Isolate defects for process improvement.

Device designs have always pushed the leading edge of technology, because the marketplace has always demanded more performance. As each wave of technology washes over the sands, new requirements are exposed whose existence beggared prior speculation.

As devices get more complex, the critical timing paths which limit them get more deeply buried and the measurements necessary to expose them become more complex still. Attempts are made to finesse the complexity by localizing the measurement; yet localized measurements can only expose defects in their predetermined locality. Worse yet, focussed performance measurements like launch-capture may compound the problem by adding confusion to the interpretation of measured internal device dynamics. Two isolated clock cycles do not behave the same way as the same two clock cycles in a continuous clock train.

Structural test strategies focus almost entirely on the third role. The raison d’étre of structural test is the blatantly wrong assumption that if the structure is correct the performance requirements will be met. The first two roles enumerated above cannot be so summarily abandoned.

If performance ATE are not used, then where is the gatekeeper? How do the IC suppliers guarantee to their customers that the devices shipped meet their requirements? The “SYSTEST” stopgap cannot be sustained in the long term - it is too expensive, too slow, too cumbersome in fault isolation, and begs the key question -- is it the device, or the system in which it is being tested, that failed?

3 Performance Measurement Requirements Can Be Met

Can the critical challenges be met?
- Pincount -- all device pins must be stressed to their margins
- Speed -- all timing paths must be exercised at speed
- Accuracy -- yield loss due to tester margins must be minimized
- DUT power -- temperature control is critical during power cycles
- DUT complexity -- the role of DFT and BIST will necessarily grow
- Vector Depth -- the required tests must be fully executed at full speed
- Pattern Generation -- can vectors be generated on the fly? APG? WRPG? Other?

Of course they can. There is no “wall” -- what there is consists of hills to climb, and with the climbing of these hills we will be able to see the structure and nature of the hills beyond them. So it has always been.

But what about the cost? Nothing is more obvious than the fact that costs required to produce will be borne. So this question really has more to do with whether the forecast costs, especially at today’s level of integration, are necessary. Do the predicted costs properly account for advances in device technology?

Cost control required to make advanced device test economical consists more in streamlining and simplifying than in abandoning device performance assurance. Some aspects of defect isolation may be too expensive to maintain in the entire fleet of production testers. Does this imply a multiple-model test fleet? If so, what is the proper mix of production versus debug capabilities? Who owns the debug requirement?