INTRODUCTION

Today we debate the potential rocks listed in the Test section of The National Technology Roadmap for Semiconductors 1997. The 1997 Test Roadmap changed dramatically the numbers presented in the 1994 Test Roadmap. We can still question the speeds, currents, DFT and pins in the Roadmap. At the same time, we question is it real and what is our future? But, it really does not matter!

VALUE OF ROADMAPS

What we need to keep in mind during this debate is the value of roadmaps to the semiconductor industry and the equipment industry that supports the semiconductor industry. Roadmaps point us in a direction. Roadmaps denote common problems and to the best ability of the authors, describe areas of research. The 1997 Test Roadmap does just this. To a large extent, the reaction of the industry to the roadmap signifies success in describing problems.

MOORE’S LAW CONTINUES

Since 1965, when first noted, transistor scaling, increased integration, faster speeds and better designs have driven our industry. It was Gordon Moore of Intel Corporation that coined the term Moore’s law. Its seemly simple extrapolation of the semiconductor industry has been the basis for all of the increased electronic content available to the consumer today (figure 1). We all benefit from Moore’s Law. We would be naive to think test equipment will stop this trend.

Figure 1 Moore’s Law- Courtesy of Intel

SOME PAST CHALLENGES

In the past walls were predicted many times. For instance it was only 10-15 years ago that lithography was forecasted to hit a wall. Optical methods were not expected to print geometries below 1.0 micron and processes were incapable of greater than 2 layers of metal. CMOS was forecasted to die a slow painful death and be replaced by SOS or GaAs technology. So what happened? First of all, the walls listed in 1985 generation roadmaps became the target of industry and academic research. Deep UV lithography, newer packages, voltage scaling, better design tools, faster test equipment all were a result of the clear needs statement in previous roadmaps.

WHAT DOES THE 1997 SIA TEST ROADMAP REALLY SAY?

Above all, the roadmap poses many challenges:

• Speeds are increasing, so, timing accuracy of testers must increase.
• CMOS power is going through the sky. Forecast of 100 Amps seem daunting today.
• Transistor density continues to increase.
• Increased interconnect, higher speeds and smaller geometries will produce defects we can hardly imagine today.

THE REAL CHALLENGES

What we need to think of as challenges is not the lines in the roadmap, but the directions, walls and methods to get around those “lines.” In much the same way as testers evolved from shared resource to per pin architecture, we need to adapt to the needs of the roadmap. Either find ways to achieve the timing, power, and costs or someone else will do it for us. That someone could be circuit design, process design or a completely new test paradigm.