Design for Soft-Error Robustness To Rescue Deep Submicron Scaling

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Progress in technological scaling allows the integration into a single chip of hundreds of millions of transistors, moving quickly to the multi-billion transistor capacities. The integration of complex systems into a single chip, that may include heterogeneous parts such as logic, SRAM, DRAM non-volatile memories, analog and even micromechanical and optical parts, is becoming a reality. Achieving acceptable reliability levels for these complex products is one of the most critical issues that need to be faced. Testability is therefore a key factor that could limit these trends if not addressed adequately. While this situation is rising many challenges in the traditional test technology domain, soft errors are becoming a major source of problems. Increased operation speeds and noise margins reduction (due to power supply reduction and geometry shrinking), that accompany the technological evolution to deeper submicron, reduce reliability of deep submicron ICs face to the various internal sources of noise. This process is now approaching a point where it will be unfeasible to produce ICs that are free from these effects. A more significant problem is related to the single-event upsets (SEUs). Recent data show that up to 20 neutrons/sq cm/hr reach the Earth's surface with an energy level greater than 10MeV. This energy level is not a real concern for today's CMOS processes. But below 0.1um, or for low supply voltage (2.2 V or less), the rates of random errors induced by cosmic neutrons will be unacceptable. These errors concern both memories and logic. Thus designing soft-error tolerant circuits is the only way to follow the path of technological scaling. Since fault tolerant design on system level results on a development and production cost that most of commodity applications can not afford, the only viable solution is to modify the design practice and CAD tools in order to generate soft-error-robust VLSI designs. As the device shrinking will progress further (e.g. 50nm, 30nm), and device behavior will become statistical (that is the device will behave correctly with a probability which is becoming increasingly different from 1), design approaches increasingly robust to soft-errors must be employed.

Among the most efficient techniques for designing soft-error tolerant circuits are: error detecting and correcting codes for memories, self-checking design for logic parts and the storage cells distributed within these parts, perturbation hardened design for latches, flip-flops, memories and logic. One or another of these techniques can be used according to the circuit case and soft-error sensitivity. Memory elements will need protection earlier, as they are the most sensitive parts. Error detecting and correcting codes (EDAC) could be used to protect memory arrays. Since this solution is very expensive for small memories and distributed storage cells, perturbation hardened storage cells (cells preserving their state under external perturbations) will be used for these parts. In a later phase, logic parts will also require protection against soft-errors as VLSI processes will move deeper to the submicron. Self-checking design is the most efficient way to protect these parts. In combination with a retry technique they allow to compute the correct result, by repeating the last operation each time a soft-error is detected. Finally, increasingly high error rates corresponding to further deep submicron scaling will require increasingly robust circuit design. In this context, perturbation hardened design for memory elements and logic will gain importance, since it can offer scalable robustness (i.e. soft-error robustness can be increased by increasing hardware cost in a continues manner), and also avoids the high interruption rates that are required for retry processing in self-checking designs, or error correction in memories with EDAC codes.

To conclude, EDAC based memory design, self-checking design, VLSI-level retry architectures, perturbation hardened design, tools for evaluation of soft error rates, and other on-line testing techniques are becoming mandatory in order to achieve increasingly levels of soft-error robustness and push aggressively the limits of technological scaling. In the next few years, considerable efforts have to be concentrated on the development of such techniques and the related CAD tools.