When Two Worlds Merge

Ken Lanier
LTX Corporation

The rapid integration of large-scale mixed-signal and digital IC designs has created entirely new demands on test engineers and test equipment manufacturers. There are three areas of most concern when considering the changes that must take place in the test community to accommodate this technology shift. These are

- test techniques,
- test equipment capabilities, and
- time to market.

Test Techniques

Test engineering has historically been split into the fairly distinct domains of digital and mixed signal. The skill sets of test engineers in these two domains have historically been very different, owing to the fact that they are generally involved in testing different types of circuits with different functions, tolerances and design margins. Even when faced with testing similar circuits, engineers with these different skill sets will implement vastly different test strategies.

At a minimum, digital and mixed signal test engineers must undergo a great deal of cross-training to become familiar with the superset of test techniques required for all the technologies which will find their way onto System-On-a-Chip (SOC) ICs.

The integration of these discrete functions into entire systems on silicon will also lead to the proliferation of new test techniques and strategies unique to larger scale devices. Debates are sure to materialize concerning the question of functional vs. component testing, the test time associated with large scale embedded memories, the definition of standard test buses, and the role of mixed-signal BIST. Standardization of test techniques and on-chip test circuitry will be required moving forward to facilitate test generation and provide sufficient test coverage in a reasonable amount of time.

Test Equipment

Test equipment is another area bound to undergo a significant transformation as a result of system-level ICs. Most large ATE manufacturers have artificially divided the test world by offering distinct digital and mixed signal test platforms. At a very basic level, this has caused test engineers to make a technical compromise when testing SOC devices since no one tester has been available until recently which contained state-of-the-art analog and digital instrumentation in one place. Having a universal test platform that contains instrumentation for all test domains will be critical to successful testing of SOC devices.

The common test platform will also facilitate lower test costs for all types of ICs tested on a given test floor. Since it is likely the higher complexity devices will require more complex test equipment and longer test times, a major factor in overall cost-of-test will be the percentage of time that a given piece of test equipment is actually utilized. Having testers dedicated to a particular type of IC means that a significant amount of capital equipment will be idle when demand for the product it tests decreases. The key to further reducing test costs is to have test equipment that can be applied to a wide array to technologies and can be easily reconfigured to address shifts in capacity requirements.

Time To Market

The time-to-market issues for system level silicon will become more problematic since the complexity of these devices will continue to increase, while the time available for test program development will continue to shrink.

In order to accommodate faster time-to-market, test software must accomplish several tasks. The first is to make the test engineer productive without having to understand the subtleties of any given piece of test equipment. The movement to provide a universal programming environment such as STIL, which presents the user with a tester-independent means of test development, must be supported and expanded to the mixed-signal realm. In addition to tester independence, tester software must better support the development and reuse of intellectual property developed in the test community. Furthermore test software must seek to balance simple test re-use with the degree of flexibility expected by mixed-signal engineers using text-based text development environments.

Lastly, mixed signal design-to-test tools will be required to facilitate the debug of SOC test programs before silicon is available. This technology is still in its early stages and will require significant amounts of standardization and integration work before it makes a significant impact on the time-to-market of system-level ICs.